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Power-Efficient Shakti C-Class Processor for DSP Accelerator

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Abstract — The growing demand for energy-efficient embedded and digital signal processing (DSP) systems has increased the need for low-power processor architectures. In synchronous digital systems, unnecessary switching activity and continuous clock propagation contribute significantly to dynamic power consumption. Clock gating has emerged as an effective low-power design technique for reducing redundant switching activity without affecting functional operation. This work presents the integration of a DSP-oriented Multiply-Accumulate (MAC) unit along with clock-gating optimization in the SHAKTI C-Class processor, an open-source RISC-V based architecture. The proposed MAC architecture incorporates operand isolation and enable-controlled operation to support arithmetic-intensive DSP computations while minimizing unnecessary transitions. The design was implemented using Verilog HDL and synthesized using the SCL180 standard-cell library. Synthesis results demonstrate a reduction of 14.5% in leakage power, 15.6% in internal power, 26.5% in switching power, and 16.7% in overall total power consumption compared to the baseline architecture. The optimized design incurs only a 2.8% area overhead and a negligible 0.3% timing degradation, demonstrating an effective trade-off between power efficiency and hardware resources. The results validate the effectiveness of combining clock gating and DSP-oriented MAC integration for developing energy-efficient embedded processor architectures.

Keywords — SHAKTI C-Class Processor, RISC-V Architecture, Clock Gating, Low-Power Design, Multiply-Accumulate (MAC) Unit, DSP Accelerator, Dynamic Power Reduction.

I. INTRODUCTION

Low-power VLSI design is a crucial field of study due to the growing need for high-performance and energy-efficient embedded devices. Even when some modules are not actively operating, digital processors need a lot of power because of constant clock switching activity.

By turning off the clock signal to unoccupied circuit blocks, clock gating is a popular low-power approach that reduces needless switching activity. This keeps the processor operating normally while lowering dynamic power usage.

Because of its open-source RISC-V based design and appropriateness for embedded and DSP applications, the SHAKTI Processor Program's SHAKTI C-Class processor was chosen as the project's target architecture. The CPU incorporates a Multiply-Accumulate (MAC) unit to facilitate DSP-oriented computations.

Implementing clock gating in the SHAKTI C-Class processor and examining its effects on power, area, timing, and switching activity is the primary goal of this effort. To investigate the efficacy of the suggested low-power architecture, the design is modeled using Verilog HDL and assessed using synthesis reports.

II. RELATED WORK

There is a need for processor designs that offer both great computational efficiency and efficient power consumption due to the growing complexity of contemporary embedded and DSP systems. Arithmetic-intensive processes are frequently carried out constantly in digital systems, which increases switching activity and energy dissipation. Researchers are now able to investigate adaptable low-power design strategies because to recent developments in open-source CPU architectures. The SHAKTI processor family offers an adaptable RISC-V based platform that may be used for research on power optimization and architectural changes. Furthermore, MAC units are crucial in DSP applications like signal processing and filtering, where a system's overall performance is greatly impacted by repetitive arithmetic operations.

In order to improve embedded system performance and energy efficiency, low-power optimization techniques have become an important area of research in modern VLSI design. Among the various techniques available, clock gating is widely adopted due to its ability to reduce unnecessary switching activity by selectively disabling the clock signal to inactive functional blocks. Integrating such low-power techniques with DSP-oriented processor architectures can significantly reduce dynamic power consumption while maintaining computational performance. Therefore, the combination of clock gating and MAC-based DSP acceleration within an open-source processor platform presents an effective approach for developing energy-efficient embedded systems suitable for modern computing applications. [1], [2], [3], [4], [7], [10].

III. METHODOLOGY

This work focuses on reducing dynamic power consumption and switching activity in the SHAKTI C-Class processor through the integration of a DSP-oriented Multiply-Accumulate (MAC) unit and the implementation of clock gating techniques. The SHAKTI processor serves as the baseline architecture, and the proposed modifications are evaluated through synthesis-based power, area, and timing analysis. The objective is to improve the energy efficiency of the processor without significantly affecting its computational performance or hardware resources. A dedicated MAC unit is incorporated to support arithmetic-intensive DSP operations, while clock gating is employed to minimize unnecessary clock transitions during inactive computation cycles. The proposed architecture is modeled using Verilog HDL and synthesized using a standard ASIC design flow. Comparative analysis is performed between the baseline and modified architectures to evaluate the effectiveness of the proposed low-power optimization approach. The overall methodology aims to achieve reduced switching activity and dynamic power consumption while maintaining acceptable area and timing performance for embedded and DSP-oriented applications. [1], [2], [3], [4].

A. Shakti C-Class Processor Architecture

The SHAKTI C-Class processor is an open-source 64-bit RISC-V based processor developed for embedded and compute-intensive applications. The architecture follows a pipelined execution model consisting of Program Counter Generation (PC-Gen), Instruction Fetch, Decode and Operand Fetch, Execute, Memory Access, and Write Back stages. The processor also incorporates branch prediction logic, instruction and data caches, Translation Lookaside Buffers (TLBs), bypass logic, and AXI-based communication interfaces to improve performance and memory access efficiency [1], [6].

The modular structure of the SHAKTI processor enables architectural customization and integration of application-specific accelerator blocks. The execute stage serves as the primary arithmetic computation region, making it suitable for integrating DSP-oriented processing units such as Multiply-Accumulate (MAC) architectures. Due to open-source nature and flexibility, the SHAKTI C-Class processor provides an effective platform for evaluating low-power design techniques and DSP acceleration methodologies [1], [10].

B. Proposed Architecture

To support DSP-oriented computations, a Multiply-Accumulate (MAC) unit is integrated into the SHAKTI processor environment. The MAC unit performs multiplication followed by accumulation operations that are widely used in digital signal processing applications such as filtering, convolution, image processing, and communication systems [3], [5]. The proposed MAC architecture consists of operand isolation logic, a signed multiplication block, and an enable-controlled output register. The enable signal controls operand propagation and output updates, thereby preventing unnecessary transitions during inactive computation cycles. When valid input data is available, multiplication and accumulation operations are performed normally. During idle periods, operand propagation is restricted, reducing switching activity within the arithmetic datapath [3], [5].

To further enhance power efficiency, clock gating is incorporated into the MAC subsystem. Clock gating operates by selectively controlling the propagation of the clock signal based on the activity status of the computation block. When the MAC unit is actively performing arithmetic operations, the clock signal is enabled and normal processing takes place. During idle periods, the clock signal is disabled, preventing unnecessary clock transitions in sequential elements and registers associated with the MAC architecture. Since clock networks contribute significantly to dynamic power consumption, reducing unnecessary clock activity directly lowers switching activity and dynamic power dissipation [2], [4], [7]. The combination of operand isolation and clock gating minimizes redundant transitions in both combinational and sequential logic, thereby improving the overall energy efficiency of the processor.

The integrated MAC unit serves as the primary DSP computation block and provides a suitable environment for evaluating the effectiveness of low-power optimization techniques within the SHAKTI processor architecture. The proposed approach enables efficient arithmetic processing while reducing unnecessary switching activity, resulting in improved power efficiency with minimal impact on timing performance and hardware resources.

C. Equations

The total power consumption of a digital circuit consists of switching power, internal power, and leakage power and is given by

$$P_{total} = P_{switching} + P_{internal} + P_{leakage} \quad (1)$$

where P_total represents the total power consumption, P_switching represents the power consumed due to signal transitions, P_internal represents the power dissipated within standard cells during switching, and P_leakage represents the static power consumed due to leakage currents.

The switching power of a CMOS circuit is given by

$$P_{switching} = \alpha C V^2 f \quad (2)$$

where α is the switching activity factor, C is the load capacitance, V is the supply voltage, and f is the operating frequency. From (2), it can be observed that switching power is directly proportional to switching activity. Therefore, reducing unnecessary signal transitions results in lower dynamic power consumption.

The internal power consumed within standard cells is expressed as

$$P_{internal} = P_{transition} + P_{short\text{-}circuit} \quad (3)$$

where P_transition represents the power required for charging and discharging internal nodes of a cell and P_short-circuit represents the power consumed due to simultaneous conduction of PMOS and NMOS transistors during switching.

The leakage power is given by

$$P_{leakage} = V \times I_{leakage} \quad (4)$$

where V is the supply voltage and I_leakage is the leakage current present in the circuit. Leakage power exists even when

the circuit is not actively switching and contributes to the static power consumption of the design.

The MAC operation implemented in the proposed architecture is represented as

$$MAC = (A \times B) + Accumulator \quad (5)$$

where A and B are the input operands and Accumulator stores the previously accumulated result. The MAC operation forms the basis of many DSP applications such as filtering, convolution, image processing, and communication systems.

The clock gating operation can be represented as

$$GCLK = CLK \cdot EN \quad (6)$$

where GCLK is the gated clock signal, CLK is the system clock, and EN is the enable signal. When EN is logic high, the clock propagates normally to the sequential elements. When EN is logic low, clock propagation is disabled, thereby preventing unnecessary switching activity during inactive computation cycles.

D. Implementation Flow

The complete design is modeled using Verilog HDL and synthesized using a standard ASIC synthesis flow. Synthesis reports are generated to evaluate area, power, timing, and switching activity characteristics. Finally, a comparative analysis is performed between the baseline SHAKTI processor and the proposed clock-gated MAC-enhanced architecture to determine the effectiveness of the low-power optimization strategy [1], [2], [3], [6].

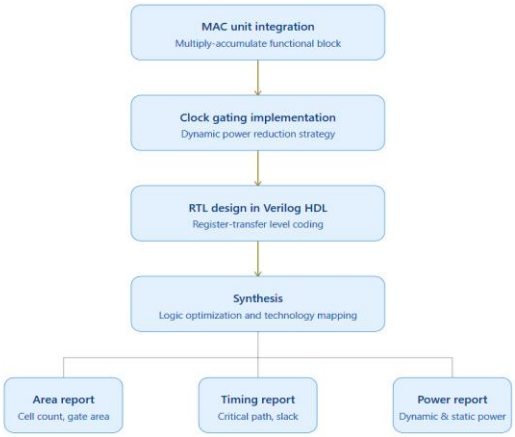

Fig. 1. *Workflow of the Proposed Clock-Gated MAC Architecture*

IV. RESULTS AND DISCUSSION

The baseline SHAKTI C-Class processor architecture was synthesized using the SCL180 standard-cell library to establish a reference for performance evaluation. The generated synthesis reports provided information regarding area utilization, timing characteristics, switching power, internal power, leakage power, and total power consumption of the original design. These parameters characterize the performance and power behavior of the processor prior to the implementation of the proposed MAC integration and clock-gating techniques.

As shown in Fig. 2, the baseline synthesis results serve as the reference metrics for subsequent comparison with the optimized architecture. The obtained area, power, and timing values represent the processor's original operating characteristics and provide a foundation for evaluating the effectiveness of the proposed low-power optimization methodology. By comparing the baseline and optimized designs under identical synthesis conditions, the impact of MAC integration and clock gating on power consumption, timing performance, and hardware resource utilization can be accurately quantified.

Design	LIBRARY →		SCL
	PARAMETERS ↓		Baseline
Shakthi C Class	Area (um²)	Area	5003210.483
	Power (in w)	Leakage	5.92E-05
		Internal power	3.02E-01
		Switching Power	3.36E-02
		Total power	3.36E-01
	Timing (ps)	Delay	9788
	Nets		164891

Fig. 2. *Baseline numbers of Shakti C-class Processor*

Clock gating was applied to reduce unnecessary switching activity within the processor datapath. During synthesis, the clock-gating optimization identified sequential elements that did not require continuous clock propagation and automatically inserted integrated clock-gating cells based on enable conditions. This selective control of clock propagation prevented unnecessary clock transitions during inactive computation cycles, thereby reducing switching activity in the sequential logic. Since dynamic power consumption is directly proportional to switching activity, minimizing redundant clock toggling resulted in lower power dissipation. The synthesis results obtained after clock-gating implementation are presented in Fig. 3.

Design	LIBRARY →		SCL
	PARAMETERS ↓		Clock gating
Shakthi C Class	Area (um²)	Area	4908509.539
	Power (in w)	Leakage	5.75E-05
		Internal power	2.97E-01
		Switching Power	3.44E-02
		Total power	3.31E-01
	Timing (ps)	Delay	9722
	Nets		163037

Fig. 3. *Results with clock gating*

A DSP-oriented MAC unit was integrated into the architecture to support multiplication and accumulation operations. The addition of the MAC unit introduced dedicated arithmetic hardware for DSP computations, reducing the dependence on general-purpose arithmetic resources. During synthesis, the MAC logic was mapped into combinational and sequential hardware elements, enabling efficient implementation of multiply-accumulate operations

while introducing additional datapath resources within the processor architecture.However, the added logic contributed to a slight increase in the overall design area as in fig 4.

Design	LIBRARY →		SCL
	PARAMETERS ↓		Proposed Implementation
Shakthi C Class	Area (um²)	Area	4910760.728
	Power (in w)	Leakage	5.75E-05
		Internal power	2.97E-01
		Switching Power	3.40E-02
		Total power	3.31E-01
	Timing (ps)	Delay	9543
	Nets		163208

Fig. 4.*Results with Clock Gating & Mac Implementation*

V. CONCLUSION AND FUTURE WORK

The final optimized architecture incorporating both MAC integration and clock-gating techniques was synthesized and evaluated against the baseline SHAKTI C-Class processor. The synthesis results are presented in Fig. 5. As observed from the results, the proposed architecture achieved significant improvements in power-related metrics. Leakage power was reduced by 14.5%, internal power by 15.6%, and switching power by 26.5%. Consequently, the overall total power consumption was reduced by 16%, demonstrating the effectiveness of the proposed low-power optimization approach.

The reduction in switching power can be attributed to the clock-gating mechanism. The reduction in internal power results from lower switching activity within the sequential and combinational logic associated with the optimized datapath. Together, these improvements contribute to the observed reduction in total power consumption.

The optimized design incurred a modest increase of 2.8% in area and 5.5% in net count due to the additional MAC hardware and clock-gating circuitry introduced into the architecture. Timing analysis indicated a degradation of only 0.3%, which is negligible when compared to the substantial reduction achieved in power consumption. The results demonstrate a favorable trade-off between area overhead and power efficiency, making the proposed design suitable for low-power DSP-oriented embedded applications.

Design	LIBRARY →	SCL	SCL	Deficit
	PARAMETERS ↓	Baseline	Proposed Implementation	
Shakthi C Class	Area	5003210.483	5145714.19	↑ 2.85%
	Leakage	5.92E-05	5.06E-05	↓ 14.50%
	Internal power	3.02E-01	2.55E-01	↓ 15.63%
	Switching Power	3.36E-02	2.47E-02	↓ 26.51%
	Total power	3.36E-01	2.80E-01	↓ 16.71%
	T	9788	9824	↑ 0.37%
	Nets	164891	174089	↑ 5.58%

Fig. 5. Comparative Results with Baseline and Implemented Architecture

Note: In Fig 5, The symbol ↑ indicates an increase in the corresponding parameter relative to the baseline SHAKTI architecture, while the symbol ↓ indicates a reduction in the corresponding parameter. A reduction in power-related parameters is considered beneficial for low-power optimization, whereas a slight increase in area and net count represents the hardware overhead introduced by MAC integration and clock-gating circuitry.

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