Machine Learning-Based Early Power Estimation of Digital VLSI Circuits Using Synthesis Parameters

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Abstract*—Machine learning-based prediction techniques have emerged as an effective solution for early estimation of VLSI design parameters, reducing the need for repeated synthesis and simulation operations. This work presents a machine learning-based framework for predicting power consumption, silicon area, and propagation delay using synthesis-oriented hardware datasets. The proposed approach employs Linear Regression, Decision Tree, Random Forest, and a combined DT+RF model using hardware-related input features including bit width, gate count, and flip-flop count. The models are trained on a dataset generated from Cadence Genus synthesis of both combinational and sequential digital circuits. Validation was performed using 8-bit, 16-bit, and 32-bit Arithmetic Logic Units (ALUs) and Up-Down Counters synthesised on the TSMC 180 nm technology library. Comparative analysis demonstrates that Decision Tree achieved the highest prediction accuracy, while Random Forest provided superior generalisation capability. The combined DT+RF model offered a balanced trade-off between accuracy and robustness. The proposed framework enables rapid early-stage VLSI parameter estimation and significantly reduces design exploration time.

***Index Terms*— VLSI, Machine Learning, Power Estimation, Area Prediction, Delay Analysis, Cadence Genus, Decision Tree, Random Forest.**

I. INTRODUCTION

Highly sophisticated digital systems with better computing performance and smaller hardware have been made possible by the quick development of Very Large Scale Integration (VLSI) technology [1]. Optimized hardware architectures with low power consumption, minimal silicon area, and decreased propagation latency are necessary for contemporary electronic devices such as embedded systems, communication processors, and artificial intelligence accelerators [2]. Achieving effective hardware optimization has grown more difficult as technology advances into nanoscale levels because of increased circuit complexity and expanding performance requirements [3]. Electronic Design Automation (EDA) tools are widely used in traditional VLSI design techniques for power estimation, timing analysis, and synthesis [4]. Repeated synthesis and simulation processes use a lot of computer resources and lengthen the design time, even though these methods yield accurate results [5]. Therefore, early hardware parameter prediction becomes crucial to lowering the complexity of design exploration and increasing optimization effectiveness. By identifying connections between hardware characteristics and circuit performance indicators, machine learning approaches offer an effective substitute for quick estimation of VLSI parameters [6]. Trained machine learning models are able to predict power, area, and delay directly from hardware-related inputs such as bit width, gate count, and flip-flop count, rather than repeating synthesis processes for each design update [7]. In the early phases of circuit design, this method facilitates quicker architectural exploration and drastically cuts down on hardware analysis time. Important VLSI design parameters are predicted in this work using supervised machine learning methods such as Linear Regression, Decision Tree, Random Forest, and a combined DT+RF model [8]. A synthesis-oriented dataset generated from Cadence Genus reports was used for model training and evaluation. To validate the proposed framework, both combinational and sequential digital circuits were considered. Arithmetic Logic Units (ALUs) and Up-Down Counters with 8-bit, 16-bit, and 32-bit architectures were synthesised using the TSMC 180 nm technology library.

II. LITERATURE REVIEW

S. Mittal and A. Kahng [1] presented a comprehensive survey on machine learning techniques for Electronic Design Automation. The work discusses the application of machine learning in various stages of VLSI design including placement, routing, timing analysis, and power optimization. The study highlights that machine learning techniques can reduce design complexity and improve hardware estimation efficiency. Z. Wang, Y. Liu, and M. Wong [2] proposed machine learning-based methods for prediction of power and timing parameters in digital circuits. Their work demonstrates that regression-based learning models can estimate circuit parameters accurately using hardware synthesis datasets. The study showed significant reduction in synthesis dependency and improved prediction speed for VLSI systems. F. Pedregosa et al. [3] introduced the Scikit-learn framework, which provides efficient implementations of machine learning algorithms such as Linear Regression, Decision Tree, and Random Forest. The framework supports preprocessing, training, testing, and evaluation of machine learning models and is widely used for prediction-oriented research applications. A. B. Kahng and S. Kang [4] discussed the role of machine learning in physical design automation. The paper focuses on optimization of placement, routing, and timing analysis using intelligent prediction techniques. The work demonstrates that machine learning methods can improve design productivity and reduce repeated hardware optimization effort.

Y. Ding, H. Ren, and P. Li [5] presented artificial intelligence-based techniques for VLSI design automation. The work explains how AI-assisted optimization can improve design exploration and hardware estimation capability in modern integrated circuits. The study also discusses the importance of data-driven methodologies for handling increasing VLSI complexity. S. Reda and A. N. Nowroz [6] proposed data-driven approaches for power estimation in integrated circuits. Their research focused on reducing computational overhead associated with repeated power analysis using conventional synthesis tools. The work demonstrated that machine learning-based prediction methods can generate reliable estimation outputs for low-power VLSI systems.
J. Cong and B. Xiao [7] discussed machine learning-based optimization techniques for hardware design. Their work emphasized intelligent prediction and optimization methods for improving hardware performance, reducing area utilization, and minimizing power consumption in digital circuits. D. Harris and S. Harris [8] explained digital design and computer architecture concepts required for understanding digital hardware systems. The book provides theoretical knowledge related to combinational circuits, sequential systems, timing analysis, and hardware implementation techniques relevant to VLSI design optimization.
I. Goodfellow, Y. Bengio, and A. Courville [9] discussed deep learning and nonlinear learning methodologies for intelligent prediction systems. Their work highlights the capability of advanced learning models to process complex datasets and generate accurate prediction outputs for engineering applications. The Cadence Genus Synthesis Solution User Guide [10] provides information regarding synthesis, timing analysis, power estimation, and area optimization in digital circuits. In the proposed work, Cadence synthesis reports are utilized for validating machine learning prediction outputs for power, area, and delay estimation. The Xilinx Vivado Design Suite User Guide [11] explains synthesis and implementation flow for digital hardware systems. The guide supports understanding of hardware design validation and FPGA-based implementation methodologies useful for VLSI optimization research.

III. METHODOLOGY

The proposed methodology employs supervised machine learning techniques to predict key VLSI design parameters, namely power consumption, silicon area, and propagation delay. The overall workflow consists of dataset preparation, preprocessing, model training, prediction, and validation. A synthesis-oriented dataset generated from Cadence Genus reports of ALU and Up-Down Counter circuits was used for training and evaluation. Hardware-related features such as bit width, gate count, and flip-flop count were used as inputs, while power, area, and delay served as target outputs. Linear Regression, Decision Tree, Random Forest, and a combined DT+RF model were implemented to estimate circuit parameters during the early stages of VLSI design.

3.1 Dataset Preparation

A synthesis-oriented dataset containing 100 circuit configurations was generated using Cadence Genus synthesis reports. The dataset included both combinational (ALU) and sequential (Up-Down Counter) circuits with 8-bit, 16-bit, and 32-bit architectures synthesised using the TSMC 180 nm technology library.

The following parameters are included in the dataset:

- Bit Width
- Gate Count
- Flip-Flop Count
- Power Consumption
- Area Utilization
- Propagation Delay
- Circuit Type

The input features consisted of Bit Width, Gate Count, and Flip-Flop Count, while Power Consumption, Area Utilisation, and Propagation Delay were considered as target outputs. The generated dataset was used for training and evaluating the machine learning models.

3.2 Dataset Preprocessing

The collected dataset was preprocessed by removing invalid entries and converting all parameters into numerical format suitable for machine learning algorithms. The dataset was divided into training and testing subsets using an 80:20 ratio. The input feature vector was defined as:

$X = [\text{Bit Width}, \text{Gates}, \text{Flip-Flops}]$

The target output vector is defined as:

$Y = [\text{Power}, \text{Area}, \text{Delay}]$

The training set is used for model learning, while the testing set is used for evaluating prediction performance.

3.3 Machine Learning Algorithm

Three supervised learning algorithms are implemented in this work for prediction of VLSI design parameters.

Linear Regression

A mathematical link between input hardware characteristics and output parameters is established using linear regression. Weighted linear combinations of input features are used by the algorithm to predict output values. For hardware parameter prediction, linear regression offers straightforward baseline estimation and is computationally efficient.

Decision Tree

Decision Tree predicts power, area, and delay parameters by recursively partitioning the dataset based on hardware-related features such as bit width, gate count, and flip-flop count. The model constructs hierarchical decision structures that effectively capture nonlinear relationships between circuit characteristics and synthesis outputs. Due to its ability to learn complex patterns directly from the data, Decision Tree provides highly accurate predictions for VLSI parameter estimation and serves as an effective model for synthesis-oriented hardware datasets.

Random Forest

Random Forest combines outputs from several decision trees using ensemble learning techniques, which improves estimation

accuracy for complex hardware datasets due to its powerful learning capability. By averaging the results from several decision trees, the final prediction is made, increasing prediction stability and decreasing overfitting. For complex hardware datasets, Random Forest's strong learning capability provides higher estimation accuracy.

The implemented models were evaluated by comparing their predicted outputs with Cadence Genus synthesis results.

3.4 Combined Prediction Method

In addition to individual model predictions, a combined DT+RF model was implemented. The final prediction was obtained by averaging the outputs of the Decision Tree and Random Forest models.

The combined forecast is shown as:

$$\text{Combined Prediction} = \frac{DT+RF}{2}$$

This approach improves prediction stability while maintaining the nonlinear learning capability of both models, resulting in more robust estimation of power, area, and delay parameters.

3.5 Evaluation Metric

The performance of the machine learning models was evaluated by comparing their predicted outputs with Cadence Genus synthesis results. The generated power, area, and delay values obtained from Linear Regression, Decision Tree, Random Forest, and the combined DT+RF model were validated against synthesis reports of ALU and Up-Down Counter circuits. This comparison was used to assess the prediction accuracy and effectiveness of the proposed machine learning framework for early-stage VLSI parameter estimation.

IV. PROPOSED ARCHITECTURE

The proposed architecture presents a machine learning-based framework for predicting power consumption, silicon area, and propagation delay during the early stages of VLSI design. The system utilises synthesis-oriented datasets generated from Cadence Genus reports of ALU and Up-Down Counter circuits. Hardware-related features such as bit width, gate count, and flip-flop count are used as inputs to Linear Regression (LR), Decision Tree (DT), Random Forest (RF), and a combined DT+RF model. The predicted outputs are validated against actual Cadence synthesis results.

Bit width, gate count, and flip-flop count are among the hardware-related input parameters that the suggested system takes. To produce estimated values for power, area, and delay, these input features are processed by machine learning models that have been trained.

Cadence synthesis reports are used to validate the generated outputs in order to assess forecast accuracy and system efficacy.

The overall architecture consists of five major stages:

- **Dataset Collection**
- **Data Preprocessing**
- **Model Training**
- **Prediction Generation**
- **Validation and Comparison**

First, various digital circuit configurations and Cadence reports are used to gather hardware parameters related to synthesis. The dataset is transformed into a numerical format appropriate for machine learning algorithms during the preparation phase, which also removes erroneous entries and missing values. During the training phase, the prepared dataset is used to train Linear Regression, Decision Tree, and Random Forest models. A combined DT+RF prediction model is then generated by averaging the outputs of Decision Tree and Random Forest. During the prediction stage, the trained models get fresh hardware input parameters following training. The machine learning algorithms generate estimated outputs for power consumption, area utilization, and propagation delay. Lastly, for validation and performance analysis, the expected outputs are contrasted with the real Cadence synthesis results.

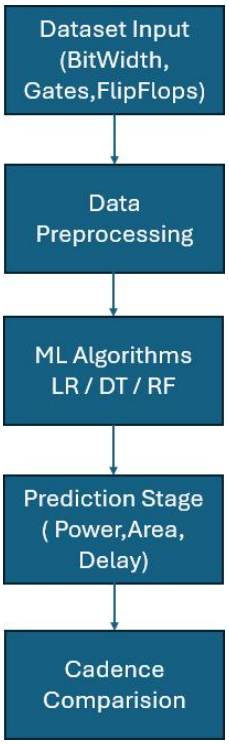

Fig.1 Proposed Machine Learning Based VLSI Prediction Flow

The full workflow of the suggested machine learning-based VLSI parameter prediction system is shown in Fig. 1. Prediction generation, model training, dataset preprocessing, and validation utilizing Cadence synthesis reports are all part of the system.

The proposed framework enables rapid estimation of VLSI design parameters without requiring repeated synthesis iterations. Validation using Cadence Genus reports of ALU and Up-Down Counter circuits demonstrates that the framework can significantly reduce design exploration time while maintaining reliable prediction accuracy.

V. RESULTS AND DISCUSSION

The proposed machine learning framework was evaluated using synthesis-oriented datasets generated from Cadence Genus reports. Validation was performed on both combinational (ALU) and sequential (Up-Down Counter) circuits with 8-bit, 16-bit, and 32-bit architectures. The predicted power, area, and delay values obtained from Linear Regression, Decision Tree, Random Forest, and the combined DT+RF model were compared against actual Cadence synthesis results.

The proposed framework accurately estimates key VLSI parameters such as power consumption, silicon area, and propagation delay. Comparative analysis indicates that different machine learning models exhibit varying levels of prediction accuracy depending on the complexity of the hardware dataset and the nonlinear relationships present in the input features.

5.1 Cadence Validation Results

The proposed machine learning framework was validated using Cadence Genus synthesis reports of ALU and Up-Down Counter circuits with 8-bit, 16-bit, and 32-bit architectures. The synthesis-generated power, area, and delay values were used as reference results for evaluating the prediction accuracy of the implemented machine learning models.

Table 1: Cadence Validation Results for ALU and Up-Down Counter Circuits

Circuit	Bit Width	Power (µW)	Area (µm^2)	Delay (ns)
ALU	8	0.0554	1486.901	2.909
ALU	16	0.1216	3163.406	5.282
ALU	32	0.2437	6270.264	10.556
Up-Down Counter	8	0.0133	944.698	1.602
Up-Down Counter	16	0.0335	1906.027	2.647
Up-Down Counter	32	0.0745	4620.370	6.325

The Cadence Genus synthesis tool was used to obtain reference power, area, and delay values for ALU and Up-Down Counter circuits implemented using the TSMC 180 nm technology library. These synthesis results serve as the ground-truth reference for validating the machine learning model predictions.

5.2 Linear Regression Analysis

For hardware parameter estimation, linear regression offers straightforward and computationally effective prediction. For linear associations found in the dataset, the model does rather well. However, compared to other machine learning models, Linear Regression exhibited comparatively larger prediction errors because of its limited ability to capture nonlinear relationships present in synthesis-oriented VLSI datasets.

Table 2: Linear Regression Prediction Results for ALU and Up-Down Counter Circuits

Circuit	Bit Width	Power (µW)	Area (µm^2)	Delay (ns)
ALU	8	0.196	593.564	2.348
ALU	16	0.362	1288.755	5.025
ALU	32	0.770	2619.770	4.362
Up-Down Counter	8	0.276	658.092	2.641
Up-Down Counter	16	0.590	1363.968	3.596
Up-Down Counter	32	1.269	2734.300	5.493

5.3 Decision Tree Analysis

Decision Tree achieved the highest prediction accuracy among the evaluated machine learning models. The model effectively captured nonlinear relationships between hardware features and synthesis outputs, producing predictions that closely matched the Cadence synthesis values for both ALU and Up-Down Counter circuits. However, Decision Tree models may be susceptible to overfitting when trained on relatively small datasets.

Table 3: Decision Tree Prediction Results for ALU and Up-Down Counter Circuits

Circuit	Bit Width	Power (µW)	Area (µm^2)	Delay (ns)
ALU	8	0.054	1438.600	2.840
ALU	16	0.126	3265.300	5.210
ALU	32	0.236	6105.700	10.180
Up-Down Counter	8	0.029	975.600	1.680
Up-Down Counter	16	0.031	1810.400	2.520
Up-Down Counter	32	0.069	4388.600	6.050

5.4 Random Forest Analysis

Random Forest achieved strong prediction performance and demonstrated superior generalisation capability through its ensemble learning approach. By combining multiple decision trees, the model reduced prediction variance and improved robustness for unseen circuit configurations. Although its prediction accuracy was slightly lower than Decision Tree for the evaluated test cases, Random Forest provided reliable and stable estimates of power, area, and delay.

Table 4: Random Forest Prediction Results for ALU and Up-Down Counter Circuits

Circuit	Bit Width	Power (µW)	Area (µm^2)	Delay (ns)
ALU	8	0.074	1398.682	2.822
ALU	16	0.138	3060.685	5.066
ALU	32	0.285	6087.502	10.214
Up-Down Counter	8	0.133	934.308	1.932
Up-Down Counter	16	0.323	1189.900	2.498
Up-Down Counter	32	0.409	3787.592	5.619

5.5 Combined Analysis

The combined DT+RF model provided a balanced trade-off between prediction accuracy and robustness. By averaging the outputs of Decision Tree and Random Forest, the model reduced prediction variations while maintaining high estimation accuracy. The combined approach produced results closer to the Cadence synthesis values than Linear Regression and demonstrated improved stability across different circuit configurations. These results indicate that the DT+RF model can be effectively used for reliable early-stage estimation of power, area, and delay in digital VLSI circuits.

Table 5: Combined Prediction Results for ALU and Up-Down Counter Circuits

Circuit	Bit Width	Power (µW)	Area (µm^2)	Delay (ns)
ALU	8	0.108	1143.675	2.670
ALU	16	0.209	2533.247	5.138
ALU	32	0.430	4937.657	8.252
Up-Down Counter	8	0.146	856.000	2.084
Up-Down Counter	16	0.315	1454.756	2.871
Up-Down Counter	32	0.582	3636.831	5.721

5.6 Comparative Analysis

Comparative analysis revealed that Decision Tree achieved the highest prediction accuracy and produced outputs that were closest to the Cadence synthesis values. Random Forest demonstrated strong prediction performance with improved robustness and generalisation capability. The combined DT+RF model provided a balanced trade-off between prediction accuracy and stability, while Linear Regression exhibited comparatively larger prediction errors. These results demonstrate the effectiveness of machine learning techniques for rapid early-stage estimation of power, area, and delay in digital VLSI circuits.

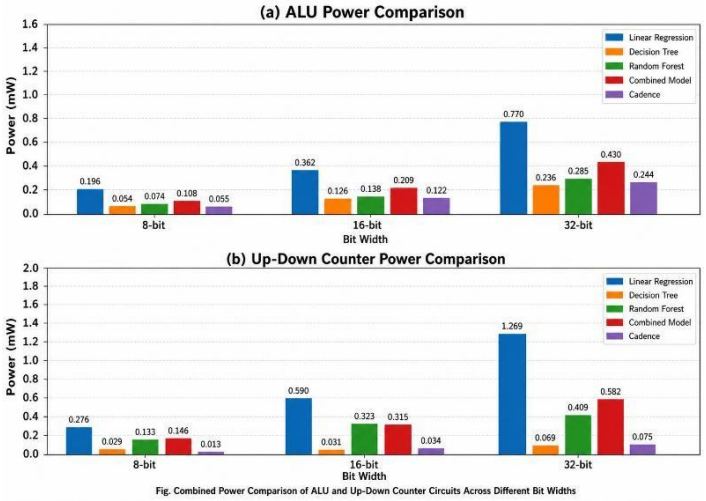

Fig. 2. Combined Power Comparison of ALU and Up-Down Counter Circuits

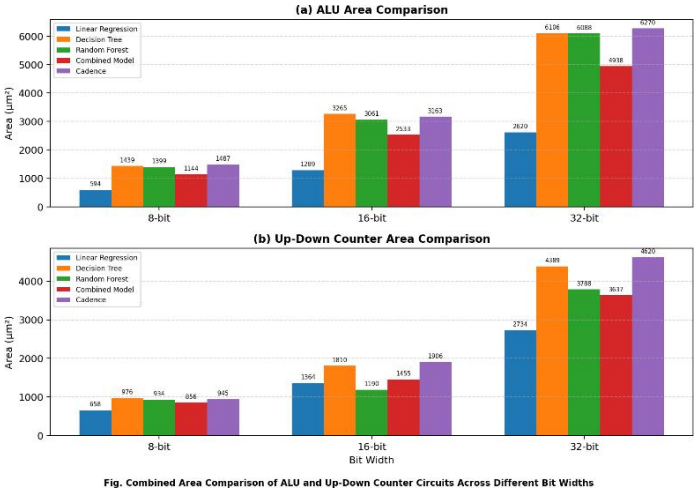

Fig. 3. Combined Area Comparison of ALU and Up-Down Counter Circuits

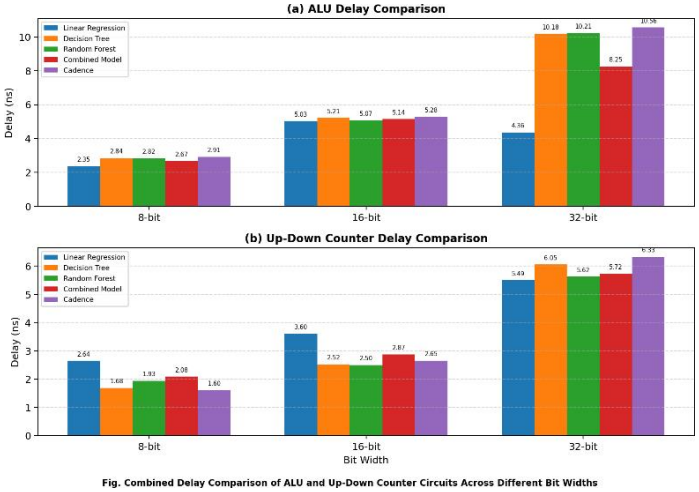

Fig. 4. Combined Delay Comparison of ALU and Up-Down Counter Circuits

VI. CONCLUSION

A machine learning-based framework for predicting key VLSI design parameters, including power consumption, silicon area, and propagation delay, was presented in this work. Synthesis-oriented datasets containing hardware-related features such as bit width, gate count, and flip-flop count were used to train and evaluate Linear Regression, Decision Tree, Random Forest, and a combined DT+RF model. Validation was performed using Cadence Genus synthesis reports of ALU and Up-Down Counter circuits with 8-bit, 16-bit, and 32-bit architectures. Comparative analysis demonstrated that Decision Tree achieved the highest prediction accuracy and produced results that were closest to the Cadence synthesis values. Random Forest exhibited strong prediction performance and superior generalisation capability for unseen circuit configurations, while the combined DT+RF model provided a balanced trade-off between prediction accuracy and robustness. Linear Regression showed comparatively larger prediction errors due to its limited ability to model nonlinear relationships present in synthesis-oriented VLSI datasets.

The proposed framework significantly reduces dependence on repeated synthesis iterations and enables rapid early-stage

estimation of power, area, and delay parameters. Future work may focus on extending the framework to larger industrial datasets, advanced technology nodes, and deep learning-based optimisation techniques. Additional VLSI parameters such as routing congestion, leakage power, thermal behaviour, and resource utilisation can also be incorporated to further enhance prediction capability.

REFERENCE

[1] S. Mittal and A. Kahng, "Machine Learning Techniques for Electronic Design Automation: A Survey," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 40, no. 6, pp. 1045–1063, 2021.

[2] Z. Wang, Y. Liu, and M. Wong, "Machine Learning-Based Power and Timing Prediction for Digital Circuits," IEEE Transactions on VLSI Systems, vol. 29, no. 11, pp. 2054–2065, 2021.

[3] F. Pedregosa et al., "Scikit-learn: Machine Learning in Python," Journal of Machine Learning Research, vol. 12, pp. 2825–2830, 2021.

[4] A. B. Kahng and S. Kang, "Machine Learning Applications in Physical Design Automation," Proceedings of IEEE ICCAD, pp. 1–8, 2021.

[5] Y. Ding, H. Ren, and P. Li, "Artificial Intelligence Techniques for VLSI Design Automation," IEEE Access, vol. 10, pp. 55321–55335, 2022.

[6] S. Reda and A. N. Nowroz, "Data-Driven Approaches for Power Estimation in Integrated Circuits," IEEE Transactions on CAD, vol. 41, no. 4, pp. 889–902, 2022.

[7] J. Cong and B. Xiao, "Machine Learning-Based Optimization for Hardware Design," IEEE Design & Test, vol. 39, no. 2, pp. 44–53, 2022.

[8] D. Harris and S. Harris, Digital Design and Computer Architecture, 3rd ed., Morgan Kaufmann, 2021.

[9] I. Goodfellow, Y. Bengio, and A. Courville, Deep Learning, MIT Press, 2021.

[10] Cadence Genus Synthesis Solution User Guide, Cadence Design Systems, 2025.

[11] Xilinx Vivado Design Suite User Guide, Xilinx Inc., 2024.

[12] K. Roy and S. Mukhopadhyay, "Low Power CMOS VLSI Design Techniques," Proceedings of the IEEE, vol. 110, no. 5, pp. 678–692, 2022.

[13] A. Krizhevsky, I. Sutskever, and G. Hinton, "Deep Neural Networks for Hardware-Aware Applications," IEEE Transactions on Neural Networks and Learning Systems, vol. 33, no. 7, pp. 3112–3124, 2022.

[14] N. Weste and D. Harris, CMOS VLSI Design: A Circuits and Systems Perspective, 5th ed., Pearson Education, 2022.

[15] M. Rabaey, A. Chandrakasan, and B. Nikolic, Digital Integrated Circuits: A Design Perspective, 3rd ed., Prentice Hall, 2021.

[16] P. Mishra and R. Kumar, "AI-Based Early Estimation of Power and Area in VLSI Systems," International Journal of Electronics and Communication Engineering, vol. 14, no. 3, pp. 201–210, 2023.

[17] H. Lee and K. Park, "Artificial Intelligence Techniques for Low Power VLSI Optimization," IEEE Access, vol. 11, pp. 15420–15431, 2023.

[18] R. Singh and A. Mehta, "Hardware Parameter Prediction Using Decision Tree and Random Forest Algorithms," IEEE International Conference on Electronics and Communication Systems, pp. 430–435, 2023.

[19] S. Gupta and M. Patel, "Performance Evaluation of Regression Models for VLSI Delay Prediction," International Journal of VLSI Design & Communication Systems, vol. 14, no. 2, pp. 33–41, 2023.

[20] A. Jain and P. Sinha, "Power Efficient Hardware Estimation Using Ensemble Learning Techniques," International Conference on Computational Intelligence and Communication Technologies, pp. 412–418, 2023.

[21] V. Sharma and R. Bhatia, "Prediction of Area and Timing Parameters in FPGA and ASIC Designs Using AI Models," IEEE International Symposium on Circuits and Systems, pp. 1–5, 2022.

[22] R. Kumar and P. Arora, "Data-Driven VLSI Optimization Using Artificial Intelligence Techniques," Journal of Electronic Testing, vol. 39, no. 1, pp. 87–98, 2023.