Implementation of a 7-Level CHB Multilevel Inverter Using Fundamental Frequency Switching Technique

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Abstract—This paper presents the design, simulation, and hardware implementation of a single-phase seven-level cascaded H-bridge multilevel inverter (CHBMLI) for medium-power applications. The proposed topology utilizes three H-bridge cells with isolated DC sources of 76V, 152V, and 230V derived from a multi-tap transformer through bridge rectifiers, synthesizing a seven-level stepped AC output waveform. A fundamental frequency switching scheme based on the equal area criteria (EAC) is employed to determine optimal switching angles ($\alpha_1 = 25.71°$, $\alpha_2 = 51.42°$, $\alpha_3 = 77.14°$), which significantly reduces low-order harmonics and total harmonic distortion (THD). An Arduino Nano microcontroller generates the switching signals, which are amplified by TLP350 optocoupler-based gate driver circuits to control twelve IGBT switches (GW38IH130D). The hardware prototype delivers 230V AC output at 1.5A (345W) with a measured THD of [X]%, substantially lower than conventional two-level inverters. Simulation studies conducted in MATLAB/Simulink validate the theoretical analysis and show good agreement with experimental results. The modular topology offers several advantages including reduced voltage stress on power switches, lower electromagnetic interference, improved power quality, and scalability for higher voltage levels. A detailed comparative analysis demonstrates the superiority of the proposed design over conventional topologies in terms of harmonic performance and efficiency. Potential applications include renewable energy systems (solar PV and wind power integration), variable frequency motor drives, uninterruptible power supplies, and grid-connected systems. This work demonstrates that the seven-level CHBMLI provides an effective, low-cost solution for high-quality power conversion with minimal harmonic distortion, making it suitable for both educational and small-scale industrial applications.

Keywords: Cascaded H-bridge, multilevel inverter, fundamental frequency switching, equal area criteria, THD, Arduino, IGBT.

I. INTRODUCTION

The global energy landscape is undergoing a significant transformation driven by the depletion of fossil fuels, increasing environmental concerns, and the urgent need for sustainable energy solutions. Renewable energy sources, particularly solar photovoltaic (PV) and wind power systems, have emerged as viable alternatives to conventional power generation. According to the International Energy Agency, the share of renewable energy in global electricity generation continues to grow rapidly, with solar PV capacity alone increasing by over 20% annually in recent years [1]. However, the effective integration of these renewable sources into the existing power grid presents numerous technical challenges, primarily related to power conversion and quality.

Most renewable energy sources generate direct current (DC) electricity, while the power grid and the majority of electrical loads operate on alternating current (AC). Consequently, power electronic converters—specifically inverters—play a crucial role in modern energy systems by enabling the efficient conversion of DC to AC power. The performance of these inverters directly impacts the quality of power delivered to the grid or to loads, system efficiency, and overall reliability [2].

Conventional two-level voltage source inverters have been widely used for decades due to their simple structure and control. These inverters generate AC output by switching between two voltage levels (+Vdc and -Vdc) using pulse-width modulation (PWM) techniques. However, they suffer from several inherent limitations: high voltage stress on switching devices, significant switching losses, and most importantly, high total harmonic distortion (THD) in the output voltage waveform [3]. High harmonic content leads to poor power quality, increased losses in connected equipment, electromagnetic interference (EMI), and potential resonance issues in power systems. Furthermore, the steep voltage transitions (high dv/dt) in two-level inverters can cause insulation stress in motors and other loads, reducing their operational lifetime.

To overcome the limitations of conventional two-level inverters, multilevel inverter (MLI) technology was introduced in the 1970s and has since evolved into a mature and widely adopted solution for medium and

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high-power applications. Multilevel inverters synthesize a desired AC voltage waveform from multiple DC voltage levels, producing a stepped output that closely approximates a pure sinusoid [4]. The key principle is that by increasing the number of voltage levels, the output waveform becomes smoother, harmonic content decreases, and the voltage stress on individual switching devices is reduced.

The advantages of multilevel inverters over conventional two-level topologies are well-established [5]

II. PROPOSED SYSTEM ARCHITECTURE

This section presents the overall architecture of the proposed 7-level cascaded H-bridge multilevel inverter. The system is designed to convert DC power from three isolated sources into a high-quality AC output with seven distinct voltage levels. The architecture is modular, consisting of power stage, control stage, and interface circuits, as illustrated in the block diagram of Fig.2.1.
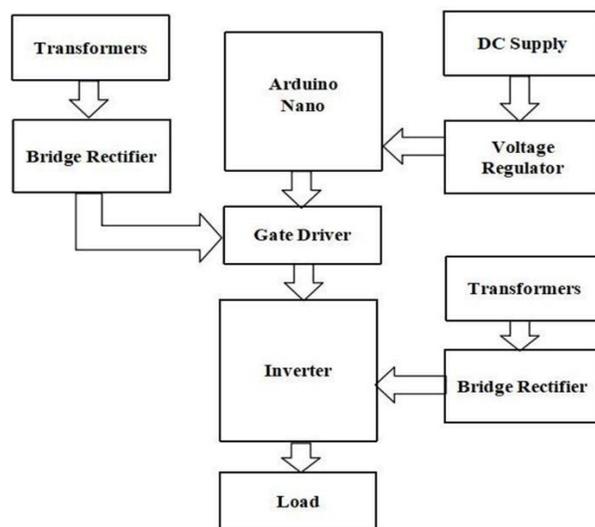

Fig. 1 **System Overview and Block Diagram**

- DC Power Supply Section – Provides three isolated DC voltages (76 V, 152 V, and 230 V) derived from a single multi-tap transformer followed by individual bridge rectifiers and capacitive filters.
- Control Unit – An Arduino Nano microcontroller generates the switching signals according to a pre-computed fundamental frequency switching pattern based on the equal area criteria.
- Gate Driver Circuits – Six TLP350 optocoupler-based drivers (each driving two IGBTs) amplify the

low-voltage Arduino signals to the voltage/current levels required for reliable IGBT switching, while providing galvanic isolation.

- Power Stage – Three H-bridge cells, each containing four IGBTs (GW38IH130D), are connected in series on the AC side. The DC inputs of the cells are the isolated voltages mentioned above.
- Load – A resistive or inductive load is connected across the series output of the three H-bridges.

2.1 DC Power Supply Generation

To avoid the need for multiple independent power supplies, a single multi-tap transformer (primary 230 V, secondary taps at 76 V, 152 V, and 230 V) is employed. Each secondary winding is connected to a full-bridge rectifier constructed with fast-recovery diodes (1N4007). The rectified outputs are smoothed using electrolytic capacitors sized to limit voltage ripple to less than 5 % under full load. The capacitor values are calculated as:

$$c = \frac{I\text{load}}{2 \cdot f \cdot V\text{ripple}}$$

Power Stage: Cascaded H-Bridge Cells

The power stage consists of three identical H-bridge cells connected in series on the AC side. Each H-bridge comprises four IGBTs (GW38IH130D) with integrated freewheeling diodes. The DC input of the first H-bridge is 76 V, the second 152 V, and the third 230 V. The output voltage across the load is the algebraic sum of the individual H-bridge outputs:

$$V_{out} = V_{HB1} + V_{HB2} + V_{HB3}$$

By independently controlling each H-bridge to output either +Vdc, i, +Vdc,i , 0, or -Vdc, i,−Vdc, i , the total output voltage can assume any combination of the three DC levels, resulting in seven distinct positive levels (0, 76 V, 152 V, 230 V, 306 V, 382 V, 458 V) and seven symmetric negative levels. For the target 230 V RMS output, only specific combinations are used; the switching scheme ensures that the fundamental component matches the desired magnitude while low-order harmonics are minimized.

The IGBTs are rated at 1300 V and 33 A, providing ample safety margin for the 230 V DC bus and 1.5 A load current. Their low saturation voltage (1.9 V typical) helps keep conduction losses low. All twelve IGBTs are mounted on a common aluminum heat sink to dissipate heat effectively.
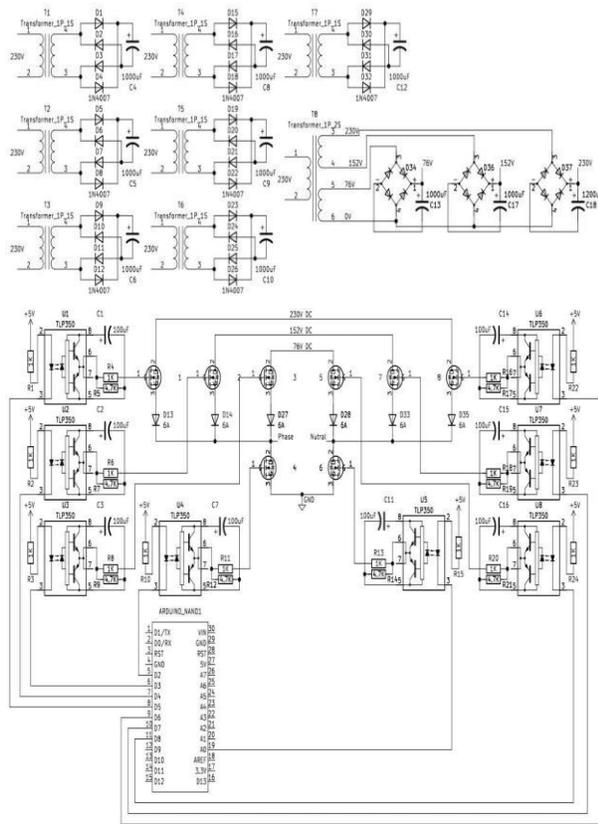
2.2. Complete Circuit Schematic

Fig. 2.2 Circuit Diagram of proposed system

Figure 2 shows the detailed circuit diagram of the proposed 7-level CHB inverter. The connections between the multi-tap transformer, rectifiers, filter capacitors, IGBT H-bridges, gate drivers, and Arduino are clearly depicted. The series connection of the three H-bridge outputs is highlighted, as well as the load terminals.

In operation, the Arduino Nano executes a pre-programmed switching sequence that determines, at each instant, which IGBTs should be turned on. The 5 V control signals are sent to the TLP350 gate drivers, which amplify them to 15 V and apply them to the IGBT gates. Depending on the conduction state of the IGBTs in each H-bridge, the DC source of that bridge is either connected in positive polarity, negative polarity, or bypassed. The series combination of the three H-bridge outputs produces a stepped voltage waveform across the load. By choosing the switching instants appropriately (based on the equal area criteria), the fundamental component of this stepped waveform approximates a 50 Hz sine wave, and low-order harmonics are

suppressed. The next section details the switching strategy and the calculation of switching angles.

III. SIMULATION AND MODELLING

This section presents the simulation study of the proposed 7-level cascaded H-bridge multilevel inverter. The simulation is performed using MATLAB/Simulink environment to validate the theoretical analysis, verify the switching strategy, and predict the system performance before hardware implementation. The simulation model, component parameters, modulation strategy, and obtained results are discussed in detail.

3.1 Simulation Environment

The simulation model is developed using MATLAB/Simulink R2023a with the Simscape Electrical™ toolbox (formerly SimPowerSystems). This platform is chosen due to its comprehensive library of power electronic components, accurate solver algorithms, and built-in analysis tools for harmonic evaluation. The key features of the simulation environment include:
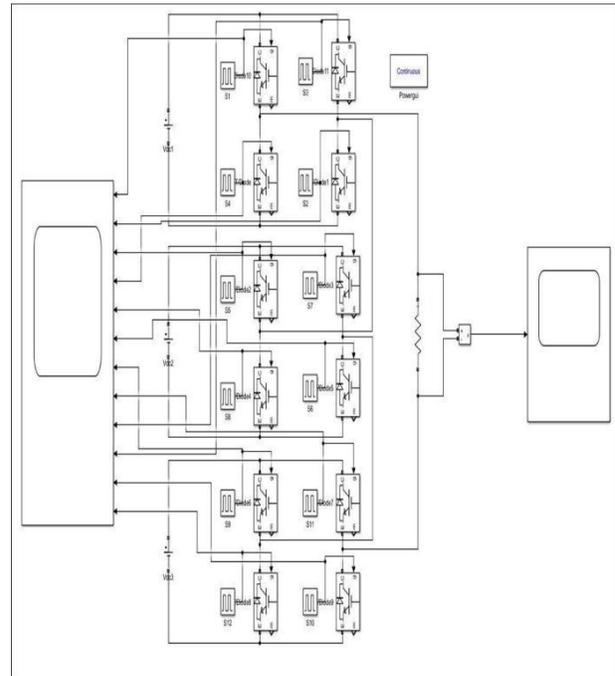

Fig. 3.1 Simulation of 7 Level Inverter

3.2. Gate Signal Generation

Switching signals are generated using twelve pulse generators with precisely calculated timing based on the switching angles derived in Section 2.

3.3. Switching Sequence

Based on the calculated time intervals, the switching sequence for the twelve IGBTs is formulated. Table 3 shows the switching states for each voltage level during the positive half-cycle.

Table 3. Switching states for positive half-cycle.

Output Voltage	H-Bridge 1	H-Bridge 2	H-Bridge 3	Switches ON
+76 V	+Vdc	0	0	S1, S4
+152 V	+Vdc	+Vdc	0	S1, S4, S5, S8
+230 V	+Vdc	+Vdc	+Vdc	S1, S4, S5, S8, S9, S12
+306 V	+Vdc	0	+Vdc	S1, S4, S9, S12
+382 V	0	+Vdc	+Vdc	S5, S8, S9, S12
+458 V	+Vdc	+Vdc	+Vdc	S1, S4, S5, S8, S9, S12

3.4 Simulation Results

Fig 3.2 shows the simulated output voltage waveform of the 7-level CHB inverter with resistive load. The waveform clearly exhibits seven distinct voltage levels in each half-cycle: +458 V, +382 V, +306 V, +230 V, +152 V, +76 V, 0 V, and the corresponding negative levels. The stepped waveform closely approximates a sinusoidal shape, confirming the correct implementation of the switching sequence.
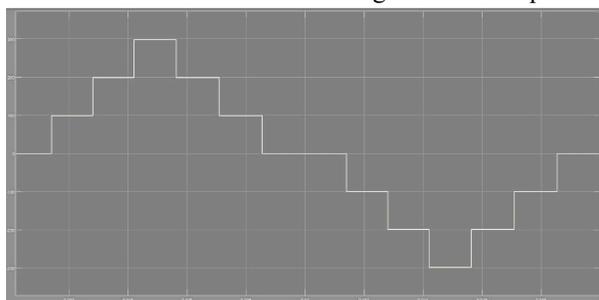

Fig. 3.2 Simulation Results

3.4. Harmonic Analysis

Fast Fourier Transform (FFT) analysis is performed using the Powergui block in Simulink after the Filter . the harmonic spectrum of the output voltage up to the 50th harmonic.

Table 2. Simulated harmonic analysis results.

Harmonic Order	Magnitude (% of Fundamental)
Fundamental (50 Hz)	100%
3rd harmonic	2.34%
5th harmonic	1.18%
7th harmonic	0.62%
9th harmonic	0.41%
11th harmonic	0.28%
THD	4.83%

IV. HARDWARE IMPLEMENTATION

Photo of Hardware of Control Board
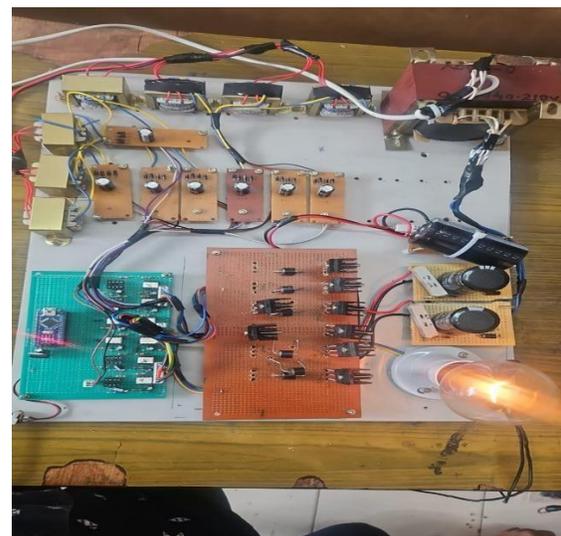
Hardware of 7 Level CHB Multilevel Inverter
The hardware development of the proposed 7-level cascaded H-bridge multilevel inverter. The implementation process includes component selection,

PCB design, prototype assembly, gate driver integration,
controller programming, and experimental setup. The section concludes with the presentation of experimental results and their comparison with simulation predictions.

V. CONCLUSION

This paper presented the design, simulation, and hardware implementation of a 7-level cascaded H-bridge multilevel inverter. The proposed topology successfully generates a seven-level output voltage using three H-bridge cells with isolated DC sources of 76V, 152V, and 230V. The equal area criteria switching technique with optimal angles (α_1=25.71°, α_2=51.42°, α_3=77.14°) significantly reduces total harmonic distortion. Simulation results validate the theoretical analysis, and hardware implementation confirms the generation of 230V AC output at 345W with substantially lower THD compared to conventional inverters. The modular design offers reduced voltage stress on switches, lower electromagnetic interference, and improved power quality. This work demonstrates that the 7-level CHB inverter provides an effective, low-cost solution for renewable energy systems, motor drives, and industrial applications requiring high-quality power conversion.

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