

# Design of Flash ADC using TIQ Technique

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**Abstract**—The majority of communication equipment in use today use analogue to digital converters. We utilize it in things like cellphones, microcontrollers, biomedical equipment, digital storage oscilloscopes, etc. We have a wide variety of Analog to Digital converters, including Dual-Slope, Flash, Pipelined, and Successive Approximation ADCs. We choose one ADC among the available ADC'S in accordance with the application's requirements. Flash ADC is used for high-speed applications requiring a wide bandwidth, although it uses more power than other analogue to digital converters. For the N-bit converter, we need  $2N-1$  comparators, and for the resistive ladder network with  $2N$  comparators, we need to cascade the high-speed comparators. We switch to a method that uses less power and does not require a resistive ladder network, which is Flash ADC utilizing the TIQ (Threshold Inverting Quantization) methodology. As the number of bits  $N$  increases, the complexity of the circuit increases. Two cascaded inverters are utilized in this method as comparators. The first inverter is used to provide internal voltages, and the second inverter serves as a gain enhancer. The TIQ approach makes use of  $2N-1$  comparators and an encoder circuit created using MUX. Using the Cadence tool, a TIQ technique-based ADC is created

**Keywords**—TIQ Comparator, MUX, Thermometer to Binary Converter)

## I. INTRODUCTION

In the current world, a data converter is needed to interact with the analogue world for modern communication and digital signal processing, and we desire DACs to recover the signal. In general, analogue to digital converters are utilized in a wide range of applications, such as storage systems, optical communication, instrumentation, high-speed serial data links, and radar communication. Analog to digital converters can be classified according to their speed, power, resolution, and complexity. The terms Dual-slope ADC, Flash ADC, Successive approximation ADC, and Pipelined ADC refer to many types of analogue to digital converters. Applications requiring low power, high speed, medium resolution, and wide band width use flash ADC. ADC has a high data conversion rate. The architecture of Flash ADC is intricate. If there are  $N$  input bits, then a resistor ladder network with  $2N$  serially connected resistors and  $2N-1$  comparator components are needed. There are  $2N-1$  comparators in the proposed ADC architecture, and a high-speed Mux-based circuit is employed to boost efficiency in place of a resistor ladder network. Threshold Inverting

Quantization Technique (TIQ) is used to create this. In this method, the first stage inverter generates internal voltages while the second stage inverter is used for voltage gain. The thermometer code is generated based on the analogue input, and the thermometer to binary code converter block converts this code to binary. The block that converts a thermometer into binary code can be created using multiplexers or adder blocks.

## II. CONVENTIONAL FLASH ADC ARCHITECTURE

Flash ADC is the fastest analogue to digital converter out of all ADCs. Direct conversion ADC is another name for this Flash ADC. Figure 1 depicts the Flash ADC block diagram. Comparators and a resistor ladder network are needed to create a Flash ADC. We need  $2N-1$  comparators and  $2N$  reference voltages, which are produced by a resistor ladder network, for a  $N$  bit ADC. Since the  $2N-1$  comparisons are performed in parallel, one clock cycle is needed. The Flash ADC conversion rate is hence high, as stated. The Flash ADC is simple to build. The design becomes more complex as the number of resistors and comparators increases with the number of bits ( $N$ ), making it unsuitable for higher numbers of bits. The number of comparators needed is almost exactly double the amount of the previous number of comparators if one bit is increased. For instance, if  $N=2$ , then  $(2*2-1=3)$  comparators are needed. If  $N=3$ , then  $(2*3-1=5)$  calls for 5 comparators.

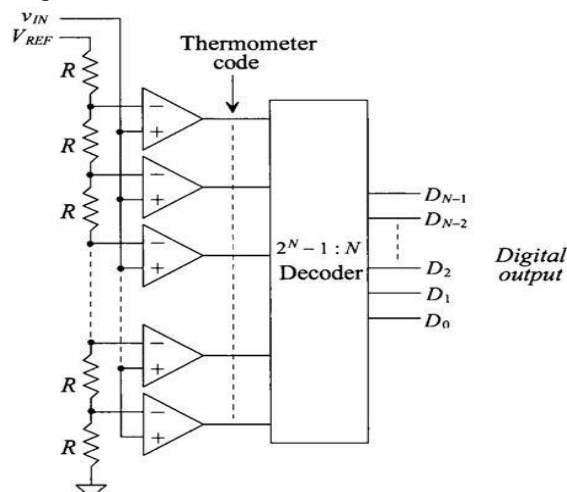


Fig.1. BLOCK DIAGRAM OF FLASH ADC

## III. PROPOSED ADC ARCHITECTURE

The suggested Flash ADC requires TIQ comparators, a temperature to binary code converter, and no resistor ladder

network. The block diagram of the suggested ADC is displayed in the diagram below.

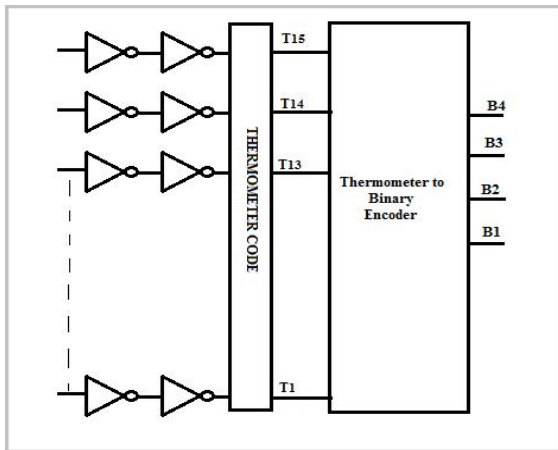


Fig.2. BLOCK DIAGRAM OF PROPOSED ADC USING TIQ TECHNIQUE

### 1.Design of 2-Bit Flash ADC

Cadence Virtuoso is used to build a 2-Bit Flash ADC, and CMOS 90nm technology is used for simulation. There are two primary building pieces for creating a 2-Bit Flash ADC. They are a temperature to binary code converter and a TIQ comparator. The internal reference voltages produced by this TIQ comparator are utilised to compare with the input voltages and produce the thermometer code. Thermometer to binary code encoder, also known as a priority encoder, is used to transform this thermometer code into binary code.

#### A.TIQ COMPARATOR

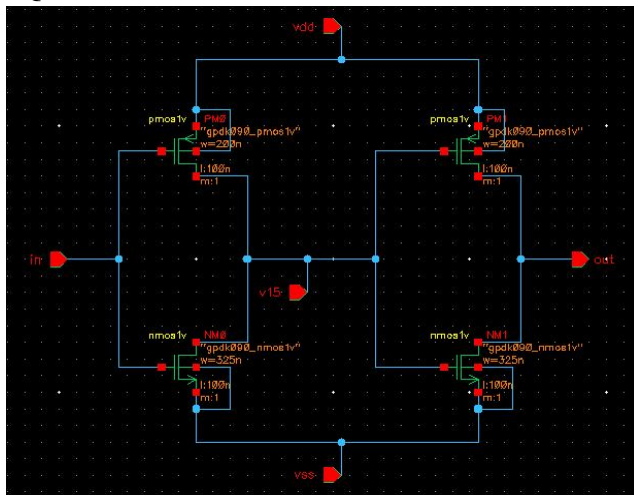


Fig.3. Schematic of TIQ comparator

Two inverters that are coupled in a cascade to create the TIQ comparator. The first of these two inverters produces the second acts as a gain stage ( $V_{in}$ ) with the transforms the input ( $v_{ref}$ ). When the input ( $v_{ref}$ ) is produced. If input voltage, logic '1' is produced. If input voltage, logic '0' is produced. The inverters can vary the reference voltages,

these voltages are employed. These voltages result from changing the width of a transistor while keeping the length constant. The expression below is used to calculate the switching voltage  $V_s$  mathematically

$$= 1 + \frac{(n-1)x^2}{1!} + \dots$$

Where  $V_{dd}$  = Supply Voltage

$V_{tp}$  = PMOS transistor threshold voltage

$V_{tn}$  = NMOS transistor threshold voltage

$K_p = u_p w_p$

$u_p$  = Holes mobility

$w_p$  = PMOS width

$K_n = u_n w_n$

$u_n$  = Electron mobility

$w_n$  = NMOS width

$W_n(\mu m)$	$W_p(\mu m)$	Switching Voltage(mv)
0.120	0.350	715.280
0.120	0.215	448.173
0.120	30	485.972

Table.1. Different voltages for different PMOS widths

#### B.ENCODER

Thermometer code is generated by the TIQ comparator, and now it is transformed to binary code using an encoder. Therefore, an encoder block is used as the next block following the TIQ comparator. An encoder can be designed using a wide variety of methods. Mux and Adders are used in the encoder's design. Less power from the aforementioned approaches is the main message. Compared to other approaches, mux-based encoders use less power.

$T_2$	$T_1$	$T_0$	$B_1$	$B_0$
0	0	0	0	0
1	0	0	0	1
1	1	0	1	0
1	1	1	1	1

Table.2.Truth table of thermometer to binary code conversion

In the above table  $T_0, T_1, T_2$  bits are thermometer code bits and  $B_0, B_1$  bits are corresponding binary bits. If the code which is generated by TIQ comparator is 110 then the corresponding binary code is 11.

3.78	0.120	472.77
5.33	0.120	488
7.53	0.120	497.38
10.62	0.120	505.30

Table.4. Different voltages for different PMOS widths

Fig.4. Schematic of 2-Bit Flash ADC

From the truth table B<sub>0</sub>,B<sub>1</sub> are the binary bits. The output of 2-Bit Flash ADC is shown in the below figure

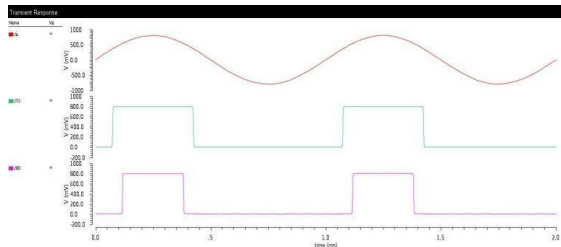


Figure.5. simulation results of 2-Bit Flash ADC

## 2.Design Of 4-Bit Flash ADC

A N-Bit Flash ADC requires  $2^N-1$  TIQ comparators. For a 4-Bits Flash ADC we require 8 comparators.

Number of bits	Number of comparators used
N-Bit	$2^N-1$
2-Bit	3 Comparators
4-Bit	8 Comparators

Table.3. Number of comparators required

As the number of bits increases the number of comparators to design the circuit are increased if the number of comparators is increases then the complexity of the circuit is increases.

### A. TIQ COMPARATOR

TIQ comparator is used to generate the internal voltages which are used as reference voltages. The different switching internal voltages are generated by keeping PMOS length constant and we vary the length. Below switching voltages are calculated by the equation given above.

W (um)	W (um)	Switching Voltage(mv)
0.120	0.120	144.69
0.169	0.120	336.69
0.239	0.120	348.39
0.338	0.120	375.92
0.477	0.120	391.32
0.673	0.120	406.38
0.950	0.120	422.54
1.34	0.120	436.46
1.89	0.120	448.69
2.67	0.120	457.62

## B. Design Of Encoder Using Full Adder

The Adders are designed by using Transistors, Transmission gates, Basic logic gates, Universal gates. By using the Transmission gate logic, it requires less power and speed is increased

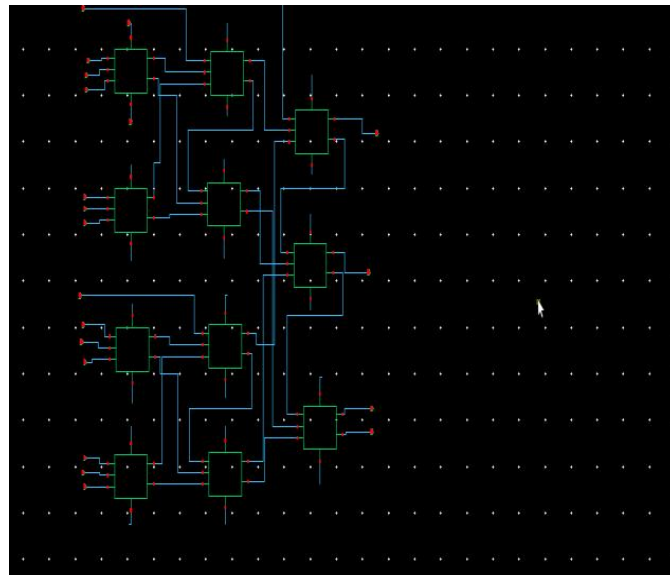


Fig.6. DESIGN OF ENCODER USING ADDERS

## C. 2X1 Based Encoder

Compared to other methods, this 2x1 Mux-based encoder uses less electricity. The input is chosen based on the selection line, and the matching output is then produced for that input. The truth table for the thermometer to binary code converter encoder is displayed in the table below.

T	T	T	T	T	T	T	T	T	T	T	T	T	T	T	B	B	B	B
1	1	1	1	1	9	8	7	6	5	4	3	2	1	0	3	2	1	0
4	3	2	1	0														
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	1
1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	0
1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	1	1	1
1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	0	0	0
1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1	0	0	1
1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	1	0	1	0
1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	1	0	1	1
1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	1	1	0	0
1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	1	1	0	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Table.5. Thermometer to binary code conversion

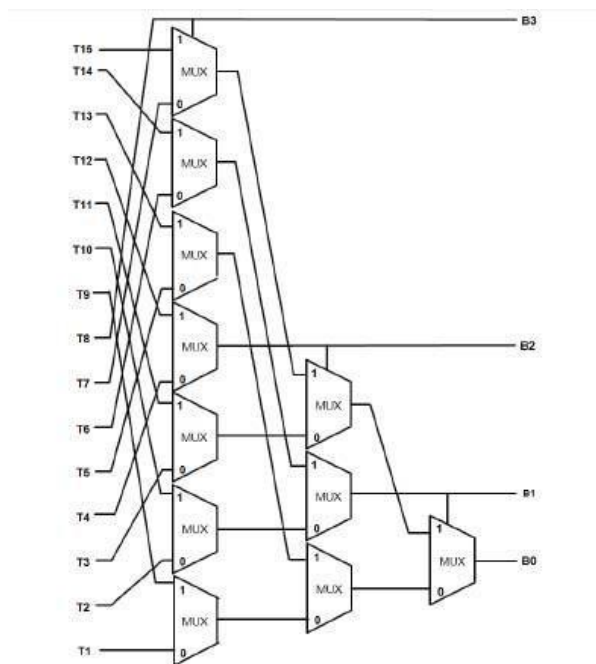


Fig.7 .2X1 Mux based encoder

The conversion of the thermometer code to binary code is seen in the aforementioned block diagram and truth table. The most important bit in this case is B3, and the least important bit is B0. We require 4 binary bits to encode 15 thermometer codes.

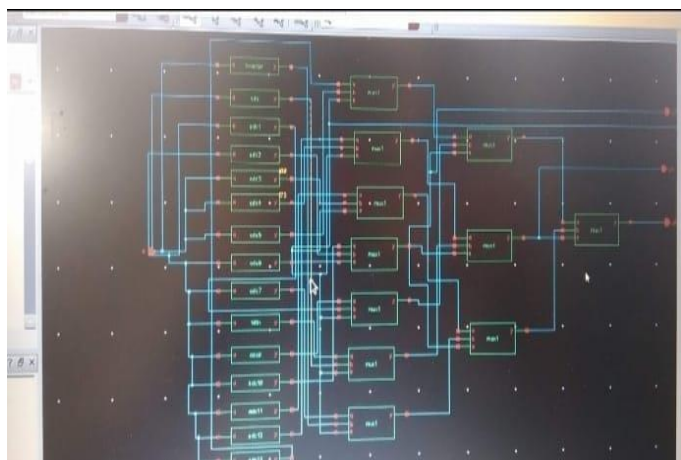


Fig.8. Schematic of 4-Bit Flash ADC

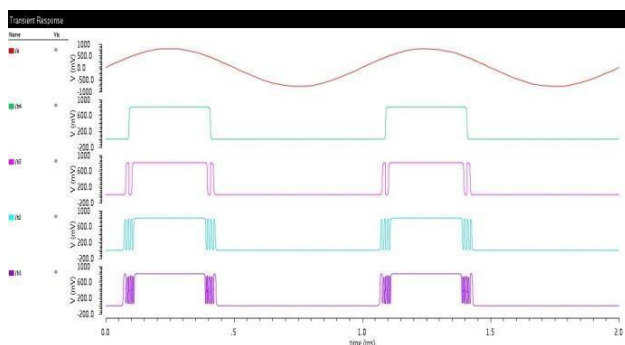


Fig.9. 4-Bit Flash ADC OUTPUT

#### IV. RESULTS

	CONVENTIONAL FLASH ADC	Adder BASED FLASH ADC	PROPOSED FLASH ADC
Technology	180nm	180nm	180nm
Resolution	4-Bit	4-Bit	4-Bit
Delay	234ns	192ns	173ns
Power Dissipation	6.72mw	10.65mw	16.58mw

The above table shows the comparison of delay and power dissipation of conventional Flash ADC and Proposed TIQ based Flash ADC.

#### V. CONCLUSION

The reduction of space and energy usage is the main focus of this essay. It is also concentrated on speed. High speed DSP processors, optical communication, and radar all use this particular method of analogue to digital conversion. In the future, power consumption will also drop if CMOS technology is improved. The reduction of space and energy usage is the main focus of this essay. It is also concentrated on speed. High speed DSP processors, optical communication, and radar all use this particular method of analogue to digital conversion. In the future, power consumption will also drop if CMOS technology is improved. Circuit complexity rose along with the number of bits used in the design. This document will be utilized in the future to expand the project to 6-Bit, 8-Bit, and 10-Bit based on various uses.

**VI. REFERENCES**

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