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Analysis of Floorplan Utilization and Routing Congestion in RTL-to-GDSII Implementation of the PicoRV32 RISC-V Core Using SKY130 Technology

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***Abstract*— This article includes an experimental investigation of the effect of floorplan utilization on routing congestion and physical implementation feasibility in the PicoRV32 RISC-V processor using the SKY130 Process Design Kit and the OpenLane open-source ASIC flow. Several RTL-to-GDSII implementation runs with floorplan usage values ranging from 50% to 70% were conducted under controlled implementation scenarios. The effects of usage scaling on core area, placement density, routing behavior, congestion increase, and implementation efficacy were thoroughly examined. The results of the trials demonstrate that excessive consumption significantly increases routing congestion and diminishes routability, whereas greater usage decreases core dimensions and enhances area efficiency. Although satisfactory implementation closure was achieved up to 60% utilization, higher use values caused significant routing congestion issues during global routing. Furthermore, implementation behavior at various placement densities was evaluated using power analysis. The study provides real usage restrictions and congestion-aware physical design insights for open-source ASIC implementation methods.**

Keywords—ASIC Physical Design, OpenLane, OpenROAD, PicoRV32, Routing Congestion, RTL-to-GDSII, SKY130

I. Introduction

The rising complexity of modern Very Large Scale Integration (VLSI) systems has made efficient physical design methods more crucial. Due to continuous transistor scaling and growing integration density, Application Specific Integrated Circuit (ASIC) implementations must adhere to specific design constraints, including silicon area, routing feasibility, timing closure, power consumption, and manufacturability. Physical design procedures that directly affect integrated circuit performance and implementation success include floorplanning, placement, Clock Tree Synthesis (CTS), and routing. Because floorplanning directly affects cell distribution, routing resource allocation, whitespace availability, and congestion behavior, it is essential to physical design.

ASIC implementation has traditionally relied heavily on commercial Electronic Design Automation (EDA) tools, which are occasionally expensive and unavailable for university research and small-scale development contexts. Recent advancements in open-source EDA frameworks such as OpenLane and OpenROAD have made it feasible to fully implement RTL-to-GDSII using publicly available Process Design Kits (PDKs). The SKY130 open-source PDK has significantly boosted research efforts in open-source ASIC creation by providing an accessible environment for physical design testing and implementation analysis. These frameworks combine the whole ASIC flow—synthesis, floorplanning, placement, CTS, routing, and signoff verification—into a single implementation sequence. [3]–[6]

PicoRV32 is a compact and lightweight RV32I RISC-V processor core that is widely used for academic research and ASIC implementation studies due to its synthesizable Register Transfer Level (RTL) architecture and reduced hardware complexity. Because of its modular architecture and open-source availability, PicoRV32 is a helpful benchmark for evaluating physical design methods and implementation behavior under various design limitations. The physical design quality of ASIC implementation procedures is greatly influenced by floorplan use, placement density, and routing resource availability. [7], [11]

Few experimental research examine the connection between floorplan use and routing congestion behavior under rising placement density conditions, despite the fact that several studies show effective RTL-to-GDSII implementation utilizing open-source ASIC flows. Although aggressive usage may greatly raise congestion, routing overflow, and implementation instability, higher utilization values promote area efficiency by decreasing core dimensions. For dependable ASIC implementation employing open-source EDA frameworks, it is consequently crucial to comprehend the practical utilization constraints for congestion-aware physical design optimization. [8] [9] [10]

An experimental congestion-aware physical design study of the PicoRV32 RISC-V core using OpenLane and SKY130 technologies is presented in this work. Under controlled implementation settings, many RTL-to-GDSII implementation runs were carried out with floorplan utilization rates ranging from 50% to 70%. A thorough analysis was conducted to determine how usage scaling affected core area, placement density, routing behavior, congestion growth, power characteristics, and implementation feasibility. While determining realistic usage limitations for effective physical implementation, experimental observations show the trade-off between routing feasibility and silicon area reduction.

The remainder of this paper is organized as follows. Section II discusses related work and existing open-source ASIC implementation studies. Section III presents the implementation methodology and experimental setup. Section IV describes the experimental results and comparative analysis. Section V discusses routing congestion behavior and failure analysis under aggressive utilization conditions. Finally, Section VI concludes the paper and outlines future research directions.

II. Related Work

Recent advancements in open-source Electronic Design Automation (EDA) frameworks have made it feasible to complete ASIC implementation procedures without depending on commercial toolchains. Open-source systems like as OpenLane and OpenROAD combine synthesis, floorplanning, placement, Clock Tree Synthesis (CTS), routing, and signoff verification into a single RTL-to-GDSII implementation environment. The publication of the SKY130 open-source Process Design Kit (PDK) has significantly enhanced research efforts in physical design experimentation and open-source ASIC creation.

Several research have successfully developed RISC-V CPU architectures using OpenLane-based design approaches. PicoRV32 has attracted a lot of attention in academic research because to its small RV32I architecture, synthesizable Register Transfer Level (RTL) design, and easier implementation. Previous studies focused mostly on timing analysis, PicoRV32 verification using SKY130 technology, and the efficient implementation of RTL-to-GDSII. These studies showed that open-source ASIC implementation procedures are feasible for lightweight RISC-V architectures, as reported in [7], [11]

Few experimental studies systematically examine the link between floorplan use and routing feasibility under increasing placement density settings, despite earlier works successfully demonstrating physical implementation utilizing open-source EDA flows. The majority of current research places more emphasis on implementation completion than on actual use limitations and congestion behavior. Routing scalability challenges were partially discussed in [8]–[10].

Thus, utilizing OpenLane and SKY130 technology, this study focuses on congestion-aware experimental investigation of PicoRV32 physical implementation by methodically changing floorplan utilization levels from 50% to 70%. The study looks into realistic routing restrictions, implementation viability, congestion increase, and utilization-dependent routing behavior in open-source ASIC design processes.

Previous studies primarily focused on successful RTL-to-GDSII implementation, timing closure, and verification of RISC-V architectures using open-source flows. However, limited attention has been given to utilization-dependent routing feasibility and congestion scalability analysis under progressively increasing placement density conditions. Furthermore, most existing studies report only final implementation success without experimentally characterizing the practical physical limits associated with aggressive floorplan compaction. [7], [8], [11], [12]

III. Methodology

The OpenLane open-source ASIC framework linked with OpenROAD and the SKY130 Process Design Kit (PDK) was used to finish the RTL-to-GDSII implementation path. Synthesis, floorplanning, placement, Clock Tree Synthesis (CTS), routing, signoff verification, and final GDSII production were all part of the implementation sequence. The PicoRV32

RTL design was synthesized using the SKY130 standard-cell library and physically implemented through automated OpenLane stages. [3]–[6]

The implementation flow used in this work is illustrated in Fig. 1.

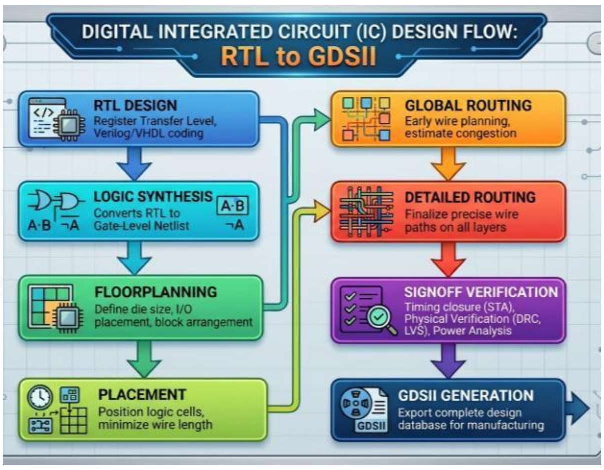

Fig. 1. Complete RTL-to-GDSII flow using OpenLane

Implementation tests were conducted under controlled physical design conditions using the same RTL, time constraints, technology libraries, and implementation flow parameters. The PicoRV32 RISC-V core was developed using SKY130A and the sky130_fd_sc_hd standard-cell library. A fixed clock duration of 10ns was used for each implementation run.

To investigate utilization-dependent congestion behavior, a number of implementation experiments were conducted by varying only the floorplan utilization parameter while maintaining the same values for all other implementation factors. Utilization values of 50%, 55%, 60%, 65%, and 70% were investigated to look at area reduction, routing behavior, congestion rise, and implementation feasibility.

TABLE I
IMPLEMENTATION PARAMETERS

Parameter	Value
Processor Core	PicoRV32
Technology	SKY130A
Design Flow	OpenLane
PDK	SKY130
Standard Cell Library	sky130_fd_sc_hd
Clock Period	10 ns
Utilization Values	50%, 55%, 60%, 65%, 70%
Operating Flow	RTL-to-GDSII

The primary objective of this work is to investigate empirically the relationship between floorplan utilization and physical implementation behavior. Floorplan utilization directly determines the portion of accessible core area that standard cells occupy during installation.

Lower utilization levels provide more whitespace and routing flexibility, but higher utilization values increase area efficiency by reducing core dimensions. However, active usage can significantly increase placement density and routing congestion.

To investigate these trade-offs, floorplan utilization was progressively increased from 50% to 70%. The implementation result, congestion behavior, routing viability, and implementation stability were recorded for each utilization level.

Using OpenROAD power estimation commands, power analysis was carried out following the successful completion of routing. The OpenROAD environment was used to evaluate the power of the routed DEF layout, combined LEF, and SKY130 liberty files. Power estimation was preceded by wire resistance-capacitance modeling and estimated parasitic extraction.

Measurements of power included:

- internal power
- switching power
- leakage power
- total power consumption

Across successful usage runs, comparative power behavior was examined.

The physical implementation behavior under various use settings was examined using the following assessment criteria.:

1. Core Area
2. Die Area
3. Placement Utilization
4. Routing Congestion
5. Routing Completion Status
6. Total Power Consumption
7. Implementation Stability

To find realistic usage limitations and congestion-aware optimization trends, these measurements were compared over several implementation runs.

IV. RESULTS AND ANALYSIS

The physical implementation behavior of the PicoRV32 RISC-V core was investigated experimentally under different floorplan utilization situations using OpenLane and SKY130 technologies. Several RTL-to-GDSII installation cycles were conducted for usage rates ranging from 50% to 70%. Comparative analysis was used to look at how usage scaling affected core area, placement density, routing behavior, congestion characteristics, power consumption, and implementation viability.

A. FLOORPLAN ANALYSIS

The link between area efficiency and implementation feasibility was examined by analyzing floorplanning behavior under various use scenarios. The design's fundamental proportions and available whitespace gradually decreased as floorplan use increased.

The solution created the biggest core area with more whitespace available at 50% usage, which led to looser placement requirements and better routing flexibility.

The experimentally observed floorplan dimensions are summarized in Table II.

TABLE II
FLOORPLAN DIMENSION ANALYSIS

Utilization	Core Area Coordinates (µm)	Die Area Coordinates (µm)
50%	5.52,10.88 to 453.56,456.96	0,0 to 459.08,469.80
55%	5.52,10.88 to 432.40,437.92	0,0 to 438.23,448.95
60%	5.52,10.88 to 414.46,418.88	0,0 to 420.04,430.76
65%	5.52,10.88 to 398.36,402.56	0,0 to 403.99,414.71

According to the experimental findings, increased consumption successfully decreased the necessary core area and enhanced silicon area efficiency. Higher usage levels, however, concurrently decreased routing flexibility and whitespace availability. Later phases of installation saw a considerable increase in congestion due to the lower routing resources during aggressive utilization levels.

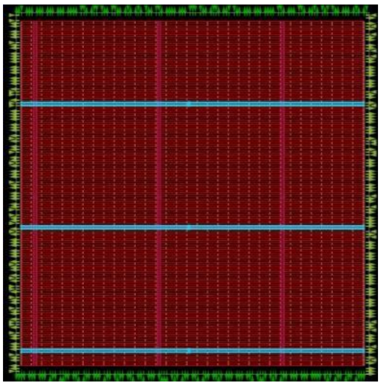

Fig. 2. Floorplan at 50% utilization

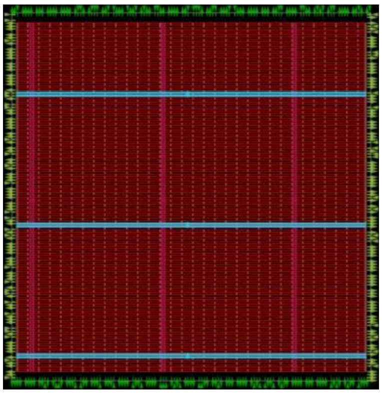

Fig. 3. Floorplan at 55% utilization

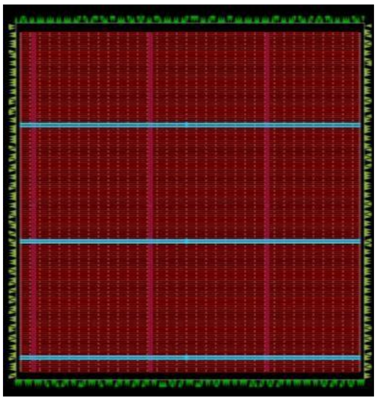

Fig. 4. Floorplan at 60% utilization

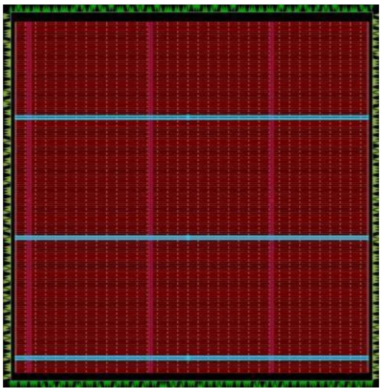

Fig. 5. Floorplan at 65% utilization

The floorplan layouts shown in Figs. 2–5 illustrate the progressive reduction in core dimensions as utilization increased from 50% to 65%.

Although higher utilization values improved area compactness, aggressive reduction in core dimensions increased placement pressure and reduced routing whitespace. This behavior established the initial conditions for congestion growth observed during placement and routing stages. Therefore, floorplan utilization directly influenced both area efficiency and implementation stability.

B. PLACEMENT ANALYSIS

The impact of floorplan use on standard-cell distribution, placement density, and congestion behavior was examined by placement analysis. The available whitespace gradually decreased as usage values rose, and placement demand inside the core region grew.

The experimentally observed placement utilization values are summarized in Table III.

TABLE III
PLACEMENT UTILIZATION ANALYSIS

Floorplan Utilization	**Observed Placement Utilization (%)**	**Placement Behavior**
50%	51.45	Relaxed placement
55%	56.44	Moderate density
60%	61.66	High density
65%	66.89	Severe congestion tendency

The placement results show that increasing floorplan utilization significantly increased effective placement density. Routing pressure increased as standard cells became more compactly distributed due to reduced whitespace availability.

Despite a noticeable rise in congestion indications, placement continued to be effective at 60% utilization. 65% utilization, which led to congestion overflow during the phases of routing optimization.

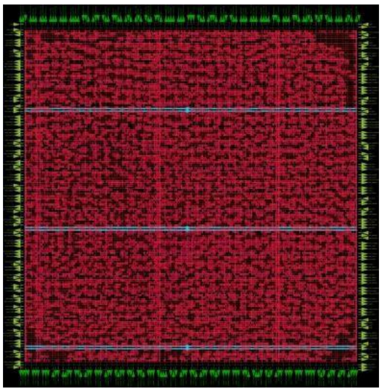

Fig. 6. Placement result at 50% utilization

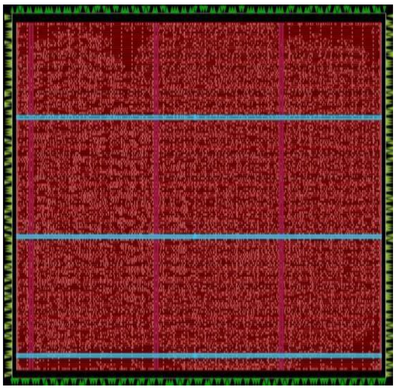

Fig.7. Placement result at 55% utilization

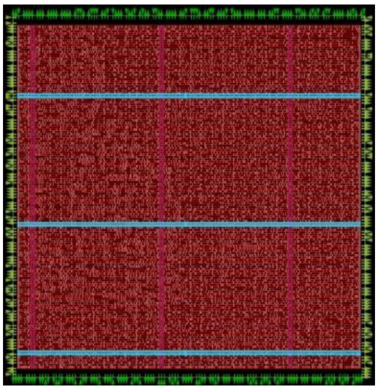

Fig.8. Placement result at 60% utilization

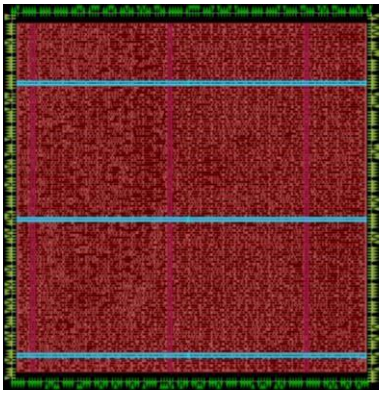

Fig.9. Placement result at 65% utilization

Utilization scaling and congestion increase are strongly correlated, according to the placement behavior. Aggressive placement compaction decreased routing flexibility and raised local routing demand, despite greater use improving silicon area efficiency. At utilization values exceeding 60%, this trade-off became more crucial.

The experimental results show that routing demand increases nonlinearly at a particular density threshold due to less whitespace and fewer routing channels, which ultimately affects implementation stability.

C. CLOCK TREE SYNTHESIS ANALYSIS

Following placement, clock signals were distributed across the constructed architecture using Clock Tree Synthesis (CTS) to maintain implementation stability under a range of use cases. The CTS stage built clock buffers based on the placement structure and established clock distribution networks for implementation runs up to 60% use. Lower utilization levels, which provided sufficient placement freedom and routing resources, led to stable CTS behavior.

Because there was less whitespace available and more placement density, routing demand around clock distribution routes increased as use rose. Even while CTS was still effective at 60% utilization, the implementation demonstrated greater congestion sensitivity in subsequent routing stages.

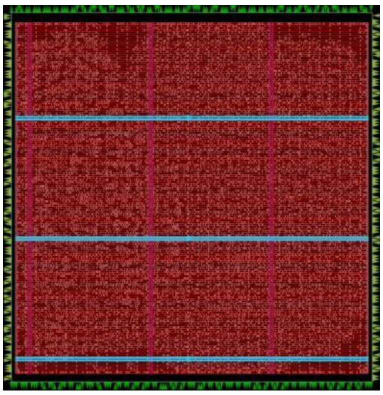

Fig. 10. CTS result at 50% utilization

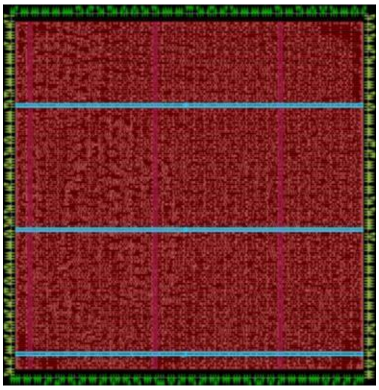

Fig. 11. CTS result at 55% utilization

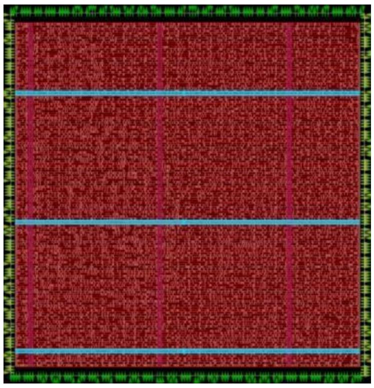

Fig. 12. CTS result at 60% utilization

Clock distribution was still feasible at moderate and high placement densities up to 60% utilization, according to the CTS data. However, routing flexibility around clock routes rapidly declined as placement compaction grew, which resulted in a rise in congestion throughout the routing optimization stages. This pattern demonstrates the interdependence between placement density and route viability in physical implementation processes.

D. ROUTING ANALYSIS

Routing research was done to look at congestion behavior and implementation viability under situations of increased floorplan utilization. Global routing and specific routing stages were analyzed to evaluate the availability of routing resources, congestion overflow, routing stability, and efficient implementation closure.

Experimental observations showed that a significant increase in routing complexity was caused by higher placement density and reduced whitespace availability. Decreased consumption levels provided sufficient routing flexibility and delivered consistent routing completion without being impacted by congestion. However, aggressive utilization levels progressively increased congestion overflow and routing strain during global routing optimization.

TABLE IV

ROUTING ANALYSIS UNDER DIFFERENT UTILIZATION CONDITIONS

Utilization	Routing Status	Congestion Behavior	Observation
50%	Successful	Low congestion	Stable routing
55%	Successful	Moderate congestion	Acceptable overflow
60%	Successful	High congestion	Routing closure achieved
65%	Failed	Severe congestion	Global routing overflow
70%	Failed	Critical congestion	Routing instability

Routing was successfully completed at 50% utilization with loose routing criteria and sufficient routing resource availability. The larger core size and additional whitespace improved the routing flexibility of the architecture and reduced local congestion pressure. It obviously indicates that there is greater room and less use.

Increasing utilization to 55% and 60% significantly increased routing complexity due to the higher placement density and fewer routing channels. Even while routing completion was still efficient at 60% utilization, congestion increased during the global and detailed routing phases.

At 65% utilization, routing congestion exceeded implementation limits. The implementation resulted in a large routing overflow during global routing optimization, which caused instability and failed routing completion.

During routing optimization, the 65% usage experiment produced global routing congestion overflow problems. The following implementation problem was noted in the routing logs:

"[ERROR GRT-0119] Routing congestion too high."

At 70% utilization, the implementation failed during placement legalization before routing execution, triggering during placement

"[ERROR GPL-0302] Placement Legalization Failure"

This behavior indicates that routing feasibility degradation is not linear with utilization scaling. Instead, congestion escalation increases rapidly after a critical density threshold due to reduced whitespace availability and routing resource exhaustion The non-linear relationship between routing feasibility and utilization scaling presents a significant risk to design closure, as congestion does not increase incrementally but rather escalates rapidly once a critical density threshold is breached.

The complete absence of unallocated whitespace prevented the standard cells from being positioned properly without overlapping, demonstrating that 60% is the highest practicable usage barrier for this particular core and technology arrangement. Due to a lack of whitespace, the placer was unable to lawfully distribute standard cells without overlap. This demonstrates that the physical routability restriction completely collapses between 60% and 65% utilization for a complicated control-logic macro such as the PicoRV32 core on a 130nm technology.

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This behavior demonstrated that aggressive use hindered successful routing convergence and drastically decreased the availability of routing resources. The unsuccessful implementation highlights the real-world routing constraints brought on by high placement density in open-source ASIC flows.

The detailed routing stage revealed increasing congestion as use numbers rose for successful implementation runs. Several optimization rounds were required to resolve routing violations in high-density routing scenarios. Detailed routing successfully converged at 60% utilization following iterative optimization, leading to zero DRC violations upon routing completion. With the appropriate LVS pass.

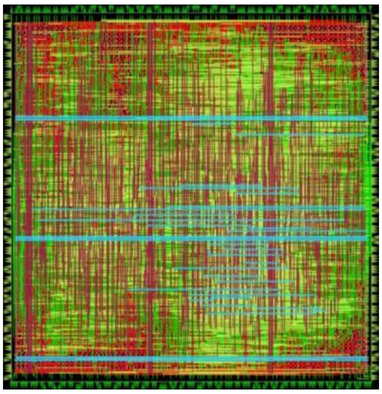

Fig. 13. Routing result at 50% utilization

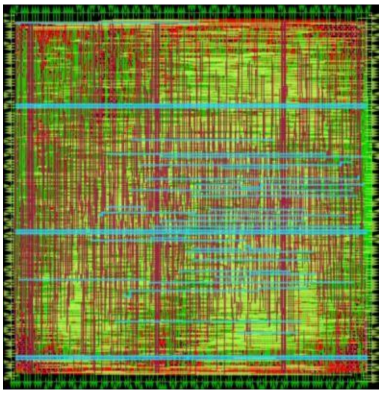

Fig. 14. Routing result at 55% utilization

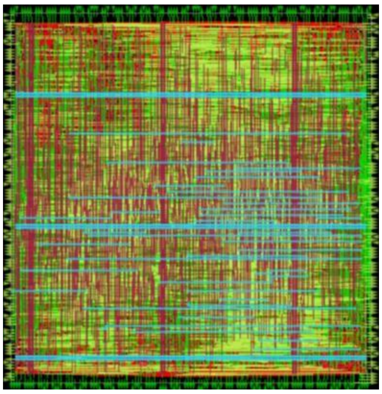

Fig. 15. Routing result at 60% utilization

The findings of the experimental routing show that above modest placement densities, routing feasibility deteriorates nonlinearly. Excessive placement compaction significantly limits routing flexibility and raises local routing demand, even when increasing use improves area compactness. When routing demand exceeds available routing resources, congestion overflow rapidly increases and implementation stability collapses.

Practical utilization limitations for congestion-aware physical implementation employing OpenLane and SKY130 technologies appear to exist based on the observed routing behavior.

E. POWER ANALYSIS

Using OpenROAD power estimation commands, power analysis was carried out following the successful completion of routing. Successful implementation runs at 50%, 55%, and 60% utilization levels were evaluated for comparative power.

The power calculation process made use of wire resistance-capacitance modeling, activity-based switching analysis, and parasitic approximation. Measurements were made of internal power, switching power, leakage power, and total power consumption.

TABLE V

POWER ANALYSIS UNDER DIFFERENT UTILIZATION VALUES

Utilization	Internal Power (W)	Switching Power (W)	Leakage Power (W)	Total Power (W)
50%	8.95e−11	8.32e−11	6.38e−08	6.40e−08
55%	8.90e−11	8.26e−11	6.19e−08	6.20e−08
60%	8.91e−11	8.14e−11	6.05e−08	6.07e−08

The findings of the experiment show that as usage rose from 50% to 60%, overall power consumption gradually decreased. Under higher placement densities, this behavior is mainly linked to shorter interconnects and more compact layouts.

Leakage power dominated the estimated total power consumption because vectorless switching activity estimation was used during OpenROAD power analysis. Therefore, the reported values primarily represent comparative implementation behavior rather than application-level runtime power

Although higher utilization improved area efficiency and slightly reduced estimated power consumption, aggressive placement compaction simultaneously increased routing congestion and implementation instability. Thus, during physical design implementation, usage optimization must strike a compromise between power efficiency and routing practicality.

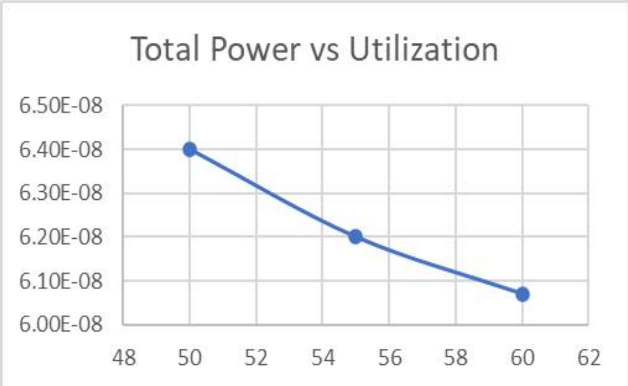

Fig. 18. Variation in total power under various utilization circumstances

The measured power behavior indicates that moderate usage scaling can improve area compactness and somewhat reduce interconnect-related power characteristics. However, congestion increases and routing instability beyond practical routing restrictions exceed the small power gains from rigorous placement compaction.

F. SIGNOFF AND GDSII GENERATION

Implementation runs successfully finished the remaining signoff stages, including layout creation, Magic view generation, LEF extraction, and GDSII construction. The OpenLane implementation process successfully produced manufacturable physical layout outputs at utilization levels up to 60%.

Complete RTL-to-GDSII implementation closure under acceptable utilization conditions was validated by the successful production of GDSII layouts.

Effective implementation convergence was hampered by routing congestion before signoff completion at higher utilization values. Therefore, congestion-aware placement conditions and routing viability were essential to the success of GDSII generation.

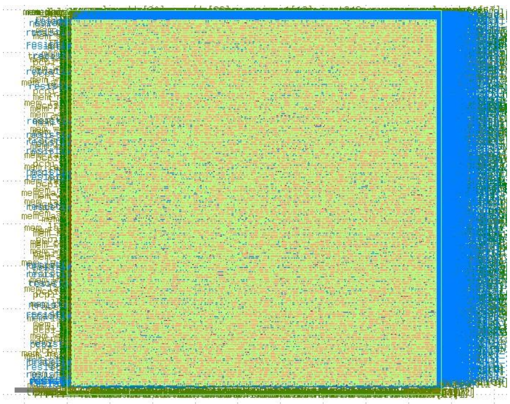

Fig. 19. Final GDSII layout at 50% utilization

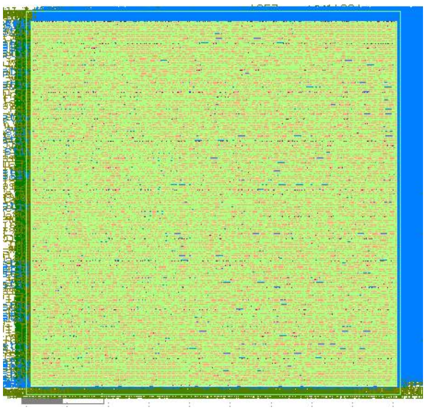

Fig. 20. Final GDSII layout at 55% utilization

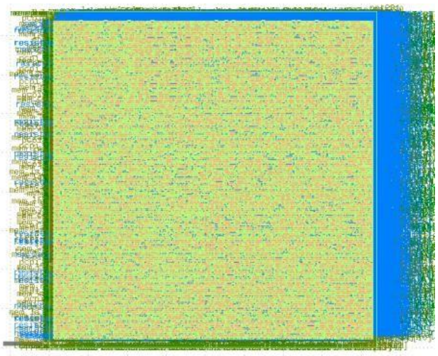

Fig. 21. Final GDSII layout at 60% utilization

The final implementation results show that although routing feasibility and consistent layout generation were maintained, effective physical implementation closure was accomplished with modest floorplan consumption values. Congestion pressure was further raised by excessive usage circumstances, which also hindered the effective completion of implementation during the routing phases.

Therefore, utilizing OpenLane and SKY130 technology, the experimental findings provide realistic usage bounds for congestion-aware ASIC implementation.

G. COMPARATIVE ANALYSIS

The link between floorplan use, placement density, routing congestion, power behavior, and implementation feasibility across many RTL-to-GDSII implementation runs was assessed using comparative analysis.

The experimental findings showed that by gradually decreasing core dimensions and layout area, boosting floorplan use enhanced silicon area efficiency. However, aggressive usage scaling reduced implementation stability by concurrently increasing placement density and routing congestion.

TABLE VI

COMPARATIVE IMPLEMENTATION ANALYSIS

Utiliz -ation	**Placement Utilization (%)**	**Routing Status**	**Conge -stion Level**	**Total Power (W)**	**Implemen -tation Result**
50%	51.45	Successful	Low	6.40e–08	Stable
55%	56.44	Successful	Mode	6.20e–08	Stable
60%	61.66	Successful	High	6.07e–08	Successful with higher congestion
65%	66.89	Failed	Severe	—	Routing overflow
70%	Failed	Critical	—	—	Implemen -tation failed

The experimental findings show that in physical implementation flows, there is a significant trade-off between area efficiency and routing feasibility. Because to the higher layout compactness, increasing usage decreased core area and somewhat better power behavior. However, during route optimization, high placement density greatly raised congestion overflow and routing demand.

Up to 60% usage, implementation closure was successful; however, greater utilization circumstances resulted in significant congestion overflow and routing instability. Routing feasibility gradually deteriorates beyond realistic placement density limitations, as shown by the observed behavior.

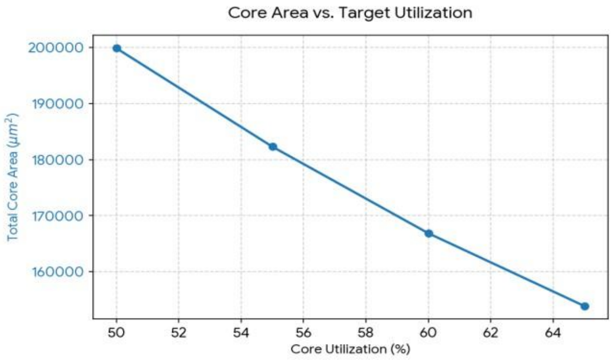

Fig. 22. Utilization versus core area reduction

The core area analysis demonstrates that increasing floorplan utilization progressively reduced the required implementation area. Higher utilization values increased placement density and reduced whitespace availability, thereby improving silicon area efficiency.

The experimental results show a clear inverse relationship between utilization and core dimensions. Although area compactness improved significantly at higher utilization values, excessive area reduction also reduced routing flexibility and increased congestion pressure during placement and routing stages.

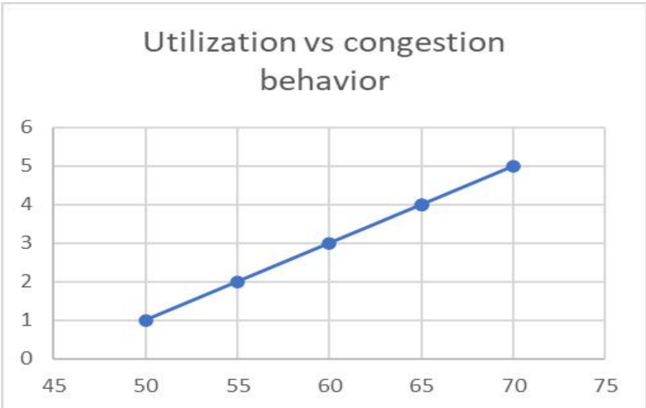

Fig. 23. Utilization versus congestion behaviour

Routing congestion gradually grew with greater usage levels, according to the congestion trend study. Stable routing behavior and less congestion strain were the outcomes of lower utilization circumstances, which offered adequate whitespace and routing freedom.

During global routing optimization, congestion grew as placement density and routing demand rose sharply with use. Additionally, the experimental data show that under aggressive use settings, congestion escalation became nonlinear. Routing demand outpaced available capacity at higher utilization values.

V. CONCLUSION

The impacts of floorplan use on routing congestion and implementation viability in the PicoRV32 RISC-V processor employing OpenLane and SKY130 technologies were investigated experimentally in this study. Several RTL-to-GDSII implementation studies were carried out with utilization circumstances ranging from 50% to 70%.

However, during physical installation, vigorous consumption greatly increased placement density and routing congestion. Reduced availability of routing resources and high congestion overflow caused routing feasibility to rapidly deteriorate beyond 60% utilization. Up to 60% utilization led to successful RTL-to-GDSII implementation closure; greater utilization circumstances resulted in routing instability and implementation failure.

As a result, the study demonstrates how crucial congestion-aware optimization is when implementing physical designs. The experimental findings verify that rather than depending exclusively on aggressive area reduction goals, physical design optimization must balance area efficiency, routing feasibility, and implementation stability.

The study that is being presented sets realistic use limits for the installation of congestion-aware open-source ASICs utilizing SKY130 technology.

FUTURE WORK

By examining sophisticated congestion-aware optimization techniques for open-source ASIC implementation processes, future research can build on this work. To increase implementation stability under high-density usage settings, timing-driven placement optimization, congestion-aware routing schemes, and adaptive floorplanning approaches might be investigated.

Machine learning-based congestion prediction models for early-stage physical design optimization may be the subject of future research. By identifying routing overflow hazards prior to detailed routing phases, these methods can improve implementation convergence and lower the complexity of design iterations.

Furthermore, in order to assess scalability, routing behavior, and physical implementation feasibility under increasing design complexity, the experimental technique described in this study may be expanded to bigger RISC-V architectures and advanced technology nodes.

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