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Advanced Low Power Static RAM Cell Design and Analysis

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Abstract—This project focuses on the development and performance analysis of an energy-efficient 7T Static RAM cell for VLSI applications. In modern digital systems, memory plays a crucial role, and Static RAM is commonly used due to its high speed and reliability. However, with continuous technology scaling, challenges such as increased power consumption, leakage current, and reduced stability have become major concerns.

The conventional 6T Static RAM cell suffers from higher leakage power and instability during read and write operations, which negatively affects overall system performance. To overcome these limitations, a 7T Static RAM cell is introduced by adding an extra transistor to the existing 6T structure. This additional transistor enhances read stability by minimizing disturbances at internal nodes and also helps in reducing leakage current.

The proposed design mainly focuses on improving the static noise margin (SNM) and reducing power dissipation, especially during the hold state. Using parameters such as power consumption, delay, and stability, the proposed 7T Static RAM cell is evaluated. The proposed design exhibits reduced power consumption and enhanced stability compared to the standard Static RAM cell. Low-power and high-performance memory applications indicate the suitability of the proposed design.

INTRODUCTION

In modern electronic systems, memory serves as a fundamental element for efficient data storage and processing. Static RAM is extensively employed in domains such as cache memory, embedded applications, digital signal processing, and portable electronic devices because of its fast operation and quick data retrieval capability. As semiconductor technology continues to advance into deep submicron regions, the requirement for energy-efficient and high-speed memory circuits has grown rapidly. However, this scaling also brings several design challenges, including increased leakage currents, higher energy dissipation, reduced operational stability, and greater sensitivity to manufacturing variations. These factors directly influence the overall performance and dependability of Static RAM cells, making power-conscious design strategies essential in present-day VLSI systems.

The standard 6T Static RAM architecture remains the most frequently implemented memory configuration due to its simplified structure and minimal area requirement. It operates using a pair of cross-coupled inverters along with two access transistors, enabling basic data storage and retrieval functions. Although this structure is efficient in terms of silicon area, it exhibits several performance limitations in scaled technologies. During the read operation, the stored information may be affected due to the direct link between internal storage nodes and bit lines, resulting in degraded stability. Furthermore, static power dissipation becomes significant during the hold condition, Even in an inactive state, the cell draws power. As the supply voltage is lowered for power reduction, the static noise margin (SNM) also declines, which can lead to reliability degradation. Due to these drawbacks, the 6T SRAM cell becomes less effective for low-power and stability-critical applications.

To address these concerns, alternative SRAM configurations such as 7T, 8T, and 9T cells have been introduced in literature. Among these, the 7T SRAM structure offers an effective compromise between power efficiency, performance, and area overhead. In this design, an additional transistor is integrated into the existing 6T framework. This modification enables separation of read and write paths, which significantly reduces read interference and improves the robustness of stored data. Moreover, it assists in regulating leakage currents, particularly during the idle or hold state, thereby contributing to lower overall energy consumption. The enhanced configuration also leads to better static noise margin, ensuring more stable operation under varying conditions.

In this work, a low-power 7T Static RAM cell is developed and examined using simulation tools. The behaviour of the proposed design is evaluated across different operating modes, including read, write, and hold conditions. Key performance indicators such as power usage, delay, and stability are considered for detailed analysis. The obtained simulation results indicate that the 7T Static RAM design outperforms the conventional 6T structure, particularly in terms of reduced leakage and improved stability. Hence, the proposed 7T Static RAM cell is a suitable candidate for modern VLSI systems, where energy efficiency and reliable operation are critical design requirements.

I. RELATED WORK

In recent years, extensive research efforts have been made to enhance Static RAM performance, particularly in terms of power efficiency and stability. The standard 6T Static RAM cell is commonly adopted due to its simple structure and small area requirement. However, with technology scaling, issues such as increased leakage current, reduced static

noise margin (SNM), and instability during read and write operations become more prominent.

These challenges become more severe in low-voltage and deep submicron technologies, making the 6T design less effective for modern low-power applications. To address these issues, various modified SRAM designs, such as 7T, 8T, and 9T cells, have been proposed. Among these, the 7T Static RAM cell provides a balanced trade-off between performance, power, and area.

In the 7T design, an extra transistor is incorporated to improve stability and reduce leakage current. This modification minimizes read disturbance and enhances data retention capability. As a result, the 7T Static RAM cell becomes a more reliable choice for low-power and high-performance VLSI applications.

A. Standard 6T Static RAM Cell Limitations

The 6T Static RAM cell is composed of two cross-coupled inverters and two access transistors. Although it provides basic read and write functionality, it suffers from read disturbance because the storage nodes are directly linked to the bit lines during read operation. This decreases stability and may lead to incorrect data reading. In addition, leakage power during hold mode is high, which increases overall power consumption. Due to these limitations, improving the 6T Static RAM design has become an important research area.

B. Need for Improved Static RAM Design

To improve upon the drawbacks of the 6T Static RAM cell, researchers have focused on modifying the existing structure rather than completely redesigning it. The main goal is to improve stability and reduce leakage power while maintaining similar area and performance. Various techniques such as adding extra transistors, separating read and write paths, and improving transistor control have been explored to enhance the Static RAM cell performance

C. Introduction of 7T Static RAM Cell

The 7T Static RAM cell is designed by modifying the Standard 6T structure with one additional transistor. This extra transistor provides better control over the circuit operation, especially during read and write processes. By modifying the structure, the 7T Static RAM cell helps in reducing read disturbance and improving data stability. The additional transistor also plays a role in controlling leakage current, which is important for low power operation.

D. Improvement in Stability and SNM

A key advantage of the 7T Static RAM cell is its improved SNM. By isolating the read path from the storage nodes, the cell achieves greater stability during read operations. This minimizes the likelihood of data flipping and improves reliability. The improved SNM makes the 7T Static RAM cell appropriate for low voltage operation and advanced CMOS technologies.

E. Reduction of Leakage Power

Leakage power has become a significant issue in modern VLSI systems. In the 7T Static RAM design, the additional transistor helps in reducing leakage current during hold mode. relative to the 6T Static RAM cell. As a result, the 7T Static RAM cell is more suitable for energy-efficient applications such as portable devices and embedded systems.

F. Motivation for 7T Static RAM Design

The main motivation for extending the 6T Static RAM cell to a 7T Static RAM cell is to enhance stability and minimize power consumption without significantly increasing the circuit area. The 7T design provides better control over read and write operations, reduces leakage current, and improves the static noise margin. These advantages make the 7T Static RAM cell a more effective option for low power and high-performance memory applications in modern VLSI systems.

II. EXISTING METHOD

A. Standard 6T Static RAM Cell (Existing Method)

The existing method considered in this work is the Standard 6T Static RAM cell, which is commonly employed in memory applications because of its simple configuration and compact layout. The 6T Static RAM cell consists of two cross-coupled inverters and two access transistors that regulate the read and write operations. During operation, the bit lines are directly linked to the storage nodes through access transistors, which allows data to be written and read from the cell.

However, the major limitation of this design is that it suffers from reduced stability during read operation and increased leakage power during the hold state. Since the storage nodes maintain a direct connection with the bit lines, the stored data can be disturbed while reading, which leads to instability and possible data loss. In addition, as technology scales down, leakage current becomes a major issue, causing continuous power dissipation even when the Static RAM cell is not actively used.

In the Standard 6T Static RAM structure, all transistors remain connected to the power supply and ground, which allows leakage current to flow continuously. This results in higher static power consumption, thereby reducing its suitability for low-power VLSI applications. Although the 6T Static RAM cell offers satisfactory performance in terms of speed and area, it does not ensure adequate stability and power efficiency in modern low-power systems. These limitations create the need for an improved Static RAM design, such as the 7T Static RAM cell, which can overcome these issues by enhancing stability and reducing leakage power.

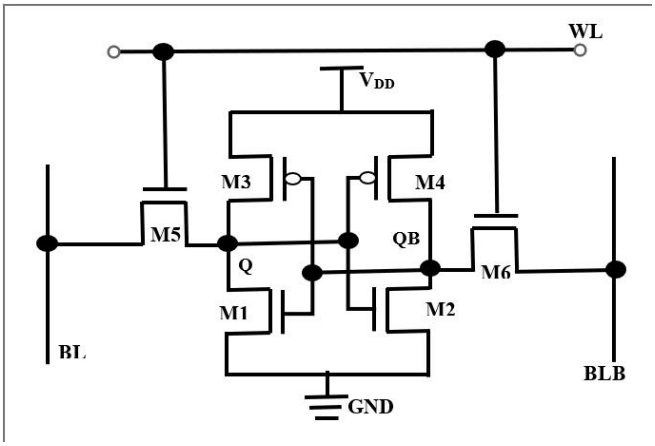

Fig.2.1 Standard 6T Static RAM Cell

The diagram depicts the transistor-level design of a conventional 6T Static RAM cell. It includes two cross-coupled inverters for data storage and two access transistors that enable read and write operations via the word line. As the bit lines are directly linked to the storage nodes, the stored data may be affected during read operations, resulting in decreased stability. The bit lines are directly connected to the storage nodes, which can disturb the stored data during read operation and reduce stability. In addition, leakage current flows through the circuit during the hold state, leading to power loss. This structure clearly highlights the drawbacks associated with the 6T Static RAM cell.

III. PROPOSED METHOD

A. Proposed 7T Static RAM Cell

The proposed method in this work is the 7T Static RAM cell, which is designed by modifying the Standard 6T Static RAM structure with an additional transistor The primary goal of this design is to enhance stability and reduce leakage power in modern VLSI applications. In the 7T Static RAM cell, an additional transistor (M7) is incorporated in the pull-down path between the storage node and ground. This additional transistor provides better control over the circuit operation, especially during read and hold conditions.

The presence of the extra transistor helps in reducing the direct connection between the storage nodes and ground, which minimizes leakage current during the hold state. It also improves the robustness of the Static RAM cell by reducing disturbance during read operation. By controlling the current flow, the 7T Static RAM cell achieves better static noise margin (SNM) relative to the Standard 6T Static RAM cell.In addition, the 7T Static RAM cell provides improved power efficiency without significantly increasing the circuit area. The separation of control using the additional transistor strengthens the reliability of the memory cell, especially in low voltage operation. Thus, in comparison with the standard 6T Static RAM design, the 7T Static RAM cell is more appropriate for applications requiring low power and high performance.

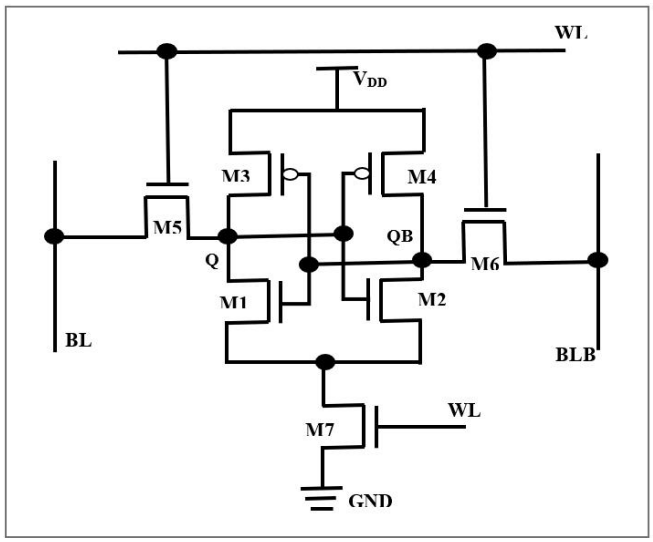

Fig.3.1. Proposed 7T Static RAM Cell

The figure depicts the transistor-level structure of the proposed 7T Static RAM cell, which is made up of two cross-coupled inverters (M1–M4), two access transistors (M5 and M6), and one additional transistor (M7). The extra transistor is positioned between the pull-down network and ground, which helps in controlling leakage current and improving stability. During operation, the word line regulates the access transistors, while the additional transistor minimizes unwanted current flow. This results in improved stability, reduced leakage power, and better overall performance relative to the 6T Static RAM cell.

IV. EXPERIMENTAL RESULTS

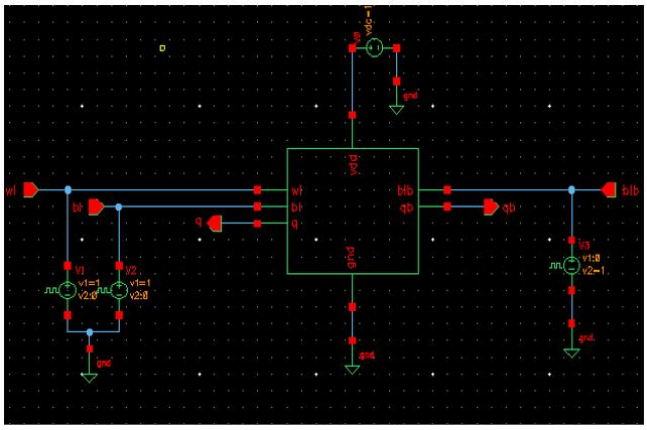

Fig. 4.1. Transient Analysis Circuits of MOSFET Based Static RAM Cells

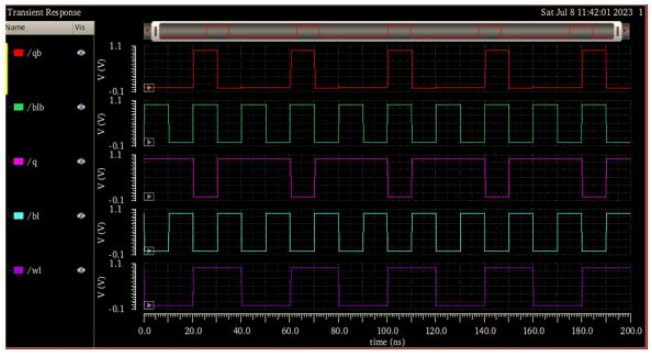

Fig.4.2. Transient Analysis Response of MOSFET Based Static RAM Cells

The illustrated diagram depicts the circuit schematic of a 7T Static RAM cell along with its transient behavior obtained through simulation using tools like Cadence. The circuit is composed of seven transistors, in which two cross-coupled inverters serve as the primary storage element and retain the data at nodes Q and QB in complementary form, meaning when Q is high, QB will be low and vice versa. The circuit consists of essential terminals such as the word line (WL), bit line (BL), and complementary bit line (BLB), which control the operation of the memory cell. The WL signal acts as a control input that enables the access transistors when it is high, permitting data to be written to or read from the cell via the bit lines. During the write operation, BL and BLB carry complementary values that are applied to the internal nodes Q and QB. The circuit is powered by VDD and grounded through GND, ensuring proper functioning of all transistors.

The transient response of this circuit shows how the voltages at different nodes such as Q, QB, WL, BL, and BLB change with respect to time during read, write, and hold operations. When WL is high, the cell becomes active and data is written into the circuit, causing Q and QB to switch to opposite logic levels. During the hold condition, when WL is low, the cross-coupled inverters maintain the stored data through their regenerative action. The waveform illustrates smooth and stable transitions, where Q and QB change exactly opposite to each other, confirming correct operation of the memory cell. Unlike the 6T Static RAM, the 7T Static RAM uses an extra transistor to isolate the read path, which reduces disturbance during operation and improves stability. As a result, the transient waveform does not show unwanted fluctuations, indicating reliable performance, faster switching, and better data retention. Therefore, both the circuit schematic and its transient response confirm that the 7T Static RAM cell provides improved stability and efficient operation for memory applications.

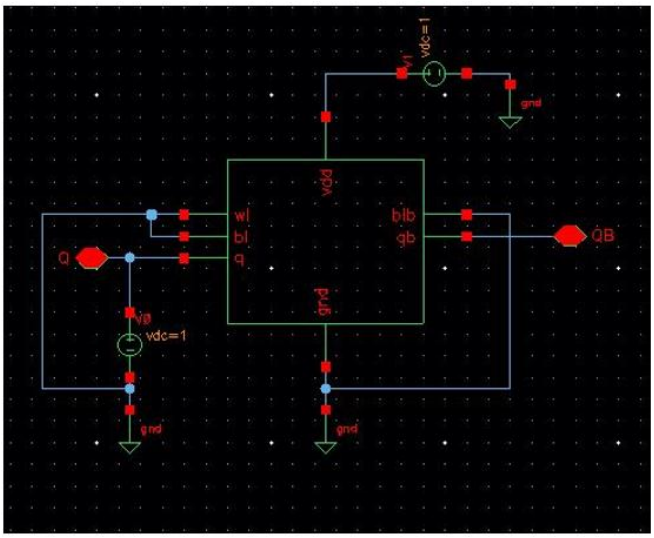

Fig. 4.3. DC Analysis Circuits of MOSFET Based Static RAM Cells

The illustrated figure depicts the schematic design of a 7T Static RAM cell implemented using the Cadence simulation tool. The storage nodes Q and QB in the circuit retain data in a complementary manner. These nodes are interconnected through cross-coupled inverters that continuously preserve the stored value. The WL is utilized to regulate the access of the cell, while the bit lines (BL and BLB) are employed to carry out read and write operations. When the WL is activated, the access transistor turns ON and enables data transfer between the internal nodes and the bit lines. The VDD and GND supply the required biasing for proper circuit operation.

An extra transistor is introduced in this design relative to the standard 6T Static RAM cell. This extra transistor assists in enhancing read stability by minimizing the disturbance at internal nodes during read operation. It also contributes to reducing leakage current and improving overall power efficiency. The circuit ensures that once a value is stored, it is reliably maintained until a new value is written.

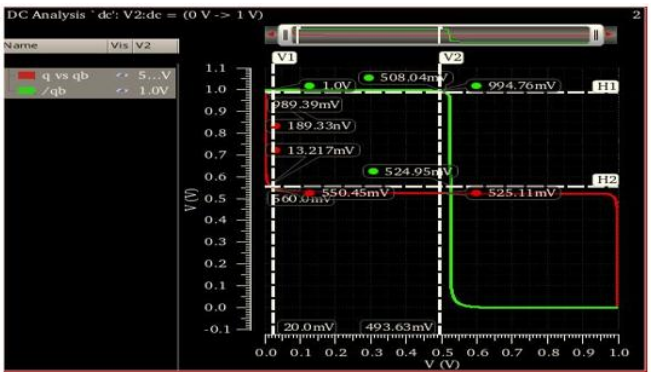

Fig. 4.4. SNM Curves of MOSFET Based Static RAM Cells

V. RESULTS AND DISCUSSION

Table.5.1. Parametric Comparison of Standard 7T Static RAM Cell and 7T Static RAM Cell with DR-VDR Technique

Parameter	7T Static RAM (Standard))	7T Static RAM (With DR-VDR)
Average Power Dissipation (nW)	1083	192.8
Leakage Power Dissipation(nW)	11.33	0.741
SNM-Hold (mV)	379.10	126.16
SNM- Write (mV)	454.04	220.99
SNM-Read (mV)	223.95	81.71
Propagation Delay (nS)	20.34	21.57
Power Delay Product (WS)	22.02×10^{-15}	4.15×10^{-15}
Average Energy Consumption (J)	44.04×10^{-15}	8.3×10^{-15}

An analysis of the performance of the proposed 7T Static RAM cell is carried out with DR-VDR technique, designed and simulated using Cadence Virtuoso, is comparatively analyzed using both DC and transient analyses. The SNM parameters (Hold, Write, and Read) are extracted from DC analysis, while the power, delay, and energy metrics are obtained from transient analysis.

From the transient analysis results, the average power dissipation is significantly reduced from 1083 nW in the standard 7T cell to 192.8 nW in the DR-VDR-based design, achieving an approximate 82.2% reduction, indicating highly efficient dynamic power optimization. Similarly, the leakage power dissipation decreases from 11.33 nW to 0.741 nW, which corresponds to an approximate 93.5% reduction, demonstrating effective suppression of standby leakage currents.

In terms of delay performance, the propagation delay shows a slight increase from 20.34 ns to 21.57 ns, representing about a 6.05% increase, which is an expected trade-off due to aggressive power reduction techniques. However, the power delay product (PDP) is drastically reduced from 22.02×10^{-15} WS to 4.15×10^{-15} WS, achieving an approximate 81.2% improvement, indicating a superior balance between speed and power efficiency. Furthermore, the average energy consumption is reduced from 44.04×10^{-15} J to 8.3×10^{-15} J, resulting in an approximate 81.15% reduction, confirming that the DR-VDR technique significantly enhances energy efficiency.

From the DC analysis perspective, the stability metrics (SNM) exhibit a reduction due to voltage scaling. The hold SNM decreases from 379.10 mV to 126.16 mV (approximately 66.7% reduction), the write SNM reduces from 454.04 mV to 220.99 mV (approximately 51.3% reduction), and the read SNM decreases from 223.95 mV to 81.71 mV (approximately 63.5% reduction). Although the SNM values are reduced, they remain within acceptable limits, ensuring reliable read, write, and hold operations under low-power conditions.

Overall, the 7T SRAM with DR-VDR technique demonstrates a substantial reduction in power, leakage, and energy consumption (above 80%), with only a minor delay penalty (~6%) and a moderate reduction in SNM due to voltage scaling. This indicates that the proposed design is highly appropriate for low-power VLSI memory applications, where energy efficiency is a critical requirement.

VI. CONCLUSION

The developed 7T Static RAM cell has been effectively implemented and evaluated, and the findings indicate that it delivers enhanced performance with respect to power consumption, stability, and energy efficiency. The simulation outcomes indicate that the standard 7T Static RAM structure exhibits strong stability with improved SNM values and dependable functionality. The addition of an extra transistor improves read stability and minimizes internal node disturbances, thereby increasing the robustness of the circuit. Moreover, the adoption of the DR-VDR technique considerably lowers power dissipation and leakage current, which are crucial parameters in low-power VLSI systems. Although there is a slight decrease in SNM along with a marginal increase in delay, the overall efficiency of the design remains acceptable for real-world usage .The lowered power-delay product and energy usage demonstrate that the proposed architecture maintains an efficient trade-off between power consumption and performance. Hence, the 7T Static RAM cell integrated with the DR-VDR technique can be regarded as an efficient and dependable memory solution for modern energy-efficient applications, including handheld gadgets, embedded platforms, and power-limited digital systems.

VII. REFERENCES

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