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Implementation of Latched Comparators in Cardiac IMDs

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Abstract:Cardiac Implantable Medical Devices are used to benefit the patients with tachycardia or bradycardia. Power consumption is important aspect of cardiac IMDs. SAR-ADC consumes most of the power which inturn reduces the battery life of the cardiac IMDs. Latched comparator in the ADC plays a major role in power consumption. Therefore it is desirable to implement a low power latched comparator. In this work we have proposed a new architecture for latched regenerative comparator which is suitable to implement in cardiac IMD applications. The proposed circuit dissipates less power when compared with the other existing architectures of latched comparators. In this paper, the proposed circuit is simulated using Tanner EDA tools in 45nm technology.

1. INTRODUCTION:

Cardiac implantable medical devices (IMD) are increasingly being used by patients to benefit from their life saving functions. These medical devices are surgically implanted into the patient's body and are configured *by*physicians. Set of techniques have implemented for controlling the heart arrhythms and failed. Finally a cardiac implantable medical device called pacemaker was first implanted in 1958 and functioned for 3 hours.A pacemaker is a small device placed in the chest or abdomen to help control abnormal heart rhythm. This device uses electrical pulses to prompt the heart to beat at normal rate. Modern pacemakers have two parts.one part, called the pulse generator contains battery and electronic circuits that control heart beat. The other part is leads which contains wires and are used to send electrical signals to the heart. These wires run from the pulse generator to the heart [1,2].

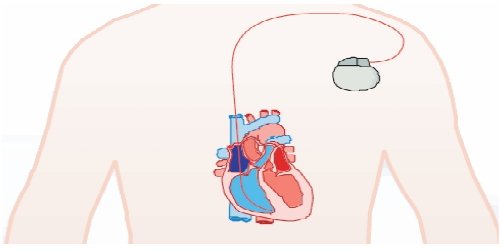

Figure 1: Cardiac implantable medical device-pacemaker

For the long survival of cardiac pacemaker, SAR ADC with low power medium speed and high accuracy must be designed. To maintain the performance of ADC with the given specifications, design of low power dynamic latched comparator is crucial Leakage currents, offset parameters and kick back noise are the various non-idealities that degrades the performance of ADC.

1.1 SAR ADCS in Implantable Medical Devices

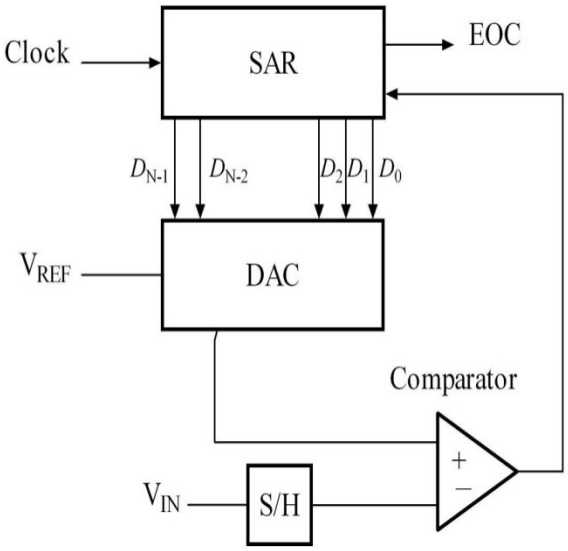

Figure 2: Block diagram of SAR ADC

SAR ADC is a type of analog to digital converter that converts a continuous analog waveform into discrete waveform. Digital output is obtained only after a binary search of all possible quantization levels. The successive approximation register is designed to supply a approximate digital code of Vin to internal DAC[3].

The Successive approximation register counts by changing the bits from MSB to LSB according to the input.Firstly,the output of SAR is converted to anolog output by DAC and this analog output is compared with the input sampled value in the comparator. This comparator provides an high or low clocked pulse based on the difference through the logic circuit.

Sample and Hold Circuit:

Sample and hold circuit is a analog device that samples the voltage of continuously varying analog signal and holds its value at constant level for specified period of time. It can hold the analog signal from few milliseconds to several seconds.

DAC:

An internal DAC compares with Vref and supplies output analog voltage to the comparator. The output of DAC will be equal to the digital code output of the SARin.

Comparator:

As we know the output of heart is digital so an analog voltage comparator is used in this project. An analog voltage comparator compares Vin and the output of internal DAC .The outputs of the comparator is fed to the successive approximation register[4].

2. Comparator Importance in SAR ADCs:

The physical cardiac signals are low frequency analog signals. Conversion of this low frequency signal doesn't require high speed but low power operation. SAR ADC is used as they are compatible with decreasing scale-down technology and can operate with low power consumption. Comparator is the crucial component of SAR ADC. Out of various design of comparators latched comparators are preferable because of its advantages.

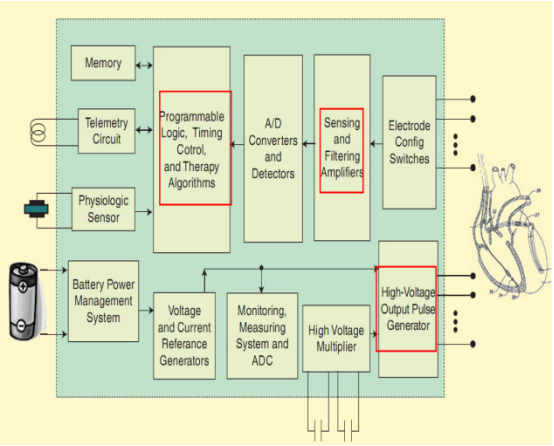

Figure 3: Comparator-fundamental building block-SAR ADC

In electronics, Operational amplifier is designed to be used with negative feedback. It can be also used as comparator in open loop configuration. On the other hand, Comparator is especially designed for open loop configuration without any feedback. Hence it is the second most widely used device in electronic circuits after Op amp. Comparators are mostly used in analog-to-digital converter (ADCs). In the conversion process, first the input signal is sampled. Then the sampled signal is applied to a number of comparators to determine the digital equivalent of the analog value. Apart from that, comparators are used in peak detectors, zero crossing detectors, BLDC operating motors, switching power regulators. Comparators is the device that compares two analog voltages or currents and switches its output to indicate which one is larger.

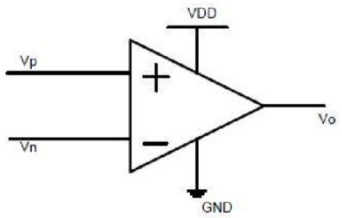

Figure 4: Schematic of comparator

If VPis at a greater potential than VP, then the output Vo of the comparator is logic 1 and when VP is at a potential less than Vn, then the output is at logic 0.If we apply a pulse voltage at VP and a DC reference voltage at Vn, the output is logic 1when the pulse amplitude is greater than the reference voltage. The figure is shown below. Thus a comparator compares two input analog value and gives binary output. In ideal case, binary signals can have two values at any point. But actually there is a transition region between
the two binary states. For a comparator, it is important to pass quickly through that transition region. Basically comparators can be divided into two types. First is the Open loop comparators, which are nothing but OP amps. The second type is regenerative comparators. Regenerative comparators use positive feedback for the comparison of magnitude between two signals[5,6].

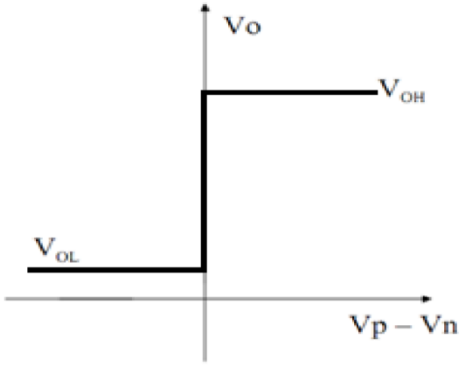

Figure 5: Voltage transfer characteristics of ideal comparator

2.1 Types of Comparators:

There are many types of comparators:

Static comparator
Dynamic comparator

Static Comparator:

Static comparators needs a dc current for its operation, but can be used as a continuous time comparator i.e., no need of a strobe signal. These are open-loop, without feedback.

Dynamic Comparator:

Dynamic comparators are widely used in the design of high-speed ADCs. Due to speed, low power consumption, dynamic latched comparators are very attractive for many applications such as high speed ADCs, memory sense amplifiers (SAs) and data receivers. Dynamic comparators doesn't require dc current , but this needs a strobe signal to latch input.

2.2 Problems of Comparator

For a cardiac implantable medical devices it is required to implement SAR ADC because it provides high accuracy and good conversion rate. The dynamic latched comparator has an important role in SAR analog to digital converter. But there are some problems which degrade the performance of the comparator. These non-idealities reduce the resolution, conversion speed and effective number of bits (ENOB) of ADCs.They are

1.Thermal Noise
2. Kickback Noise
3. Offset Voltage

Thermal Noise:

Generally thermal noise is a limiting factor for achieving a good resolution of several ADC architecture with scaled supply voltages. In dynamic comparators the thermal noise can be reduced by increasing the number of MOS transistors. But this increase leads to the generation of kickback noise.

Offset Voltage:

- The offset voltage is a parameter defining the differential DC voltage required between the inputs of an amplifier.
- Offset in the comparators are generated due to input transistor mismatches.

Input Offset Voltage:

The input offset voltage is the voltage which must be applied between the two input terminals to balance the amplifier.

Output Offset Voltage:

The Output Offset Voltage is defined as the DC voltage present at the output terminal of the comparator when the two input terminals are grounded.

Kickback Noise:

Kickback noise is generated in the architectures of latched comparators on wide range of voltage variations. The circuit diagram of generation of kickback noise is as shown in below figure.

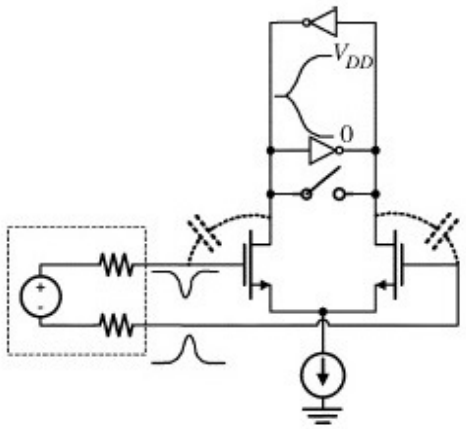

Figure 6: Generation of kickback noise

2.3 Working of Latched Comparators

Latched comparators operates in two modes. They are

- **Reset Mode**
- **Comparison Mode**

Reset Mode:

In reset mode CLK=0.when CLK=0 the switch is closed and the transistor current depends on input voltage which results in the small output voltage due to non -zero resistance of the switch.

Comparison Mode:

In this mode,CLK=1 OR VDD.when CLK=1 switch is open and the two cross coupled inverters implement a positive feedback. This makes the output voltage go towards 0 and VDD.

The large variations in the voltage on the regeneration nodes are coupled through parasitic capacitance of the transistors. Since the circuit does not have zero output impedance, the input voltage is disturbed which may degrade the accuracy of converter. This disturbance is called KICKBACK noise.

2.4 Existing Architectures:

The most popular technique for reducing the kickback noise in latched regenerative comparator is to add a pre amplifier circuit before the latched stage in the comparator.Although this technique reduces the power efficiency of latched comparator by introducing static consumption of power ,we go for neutralization technique.

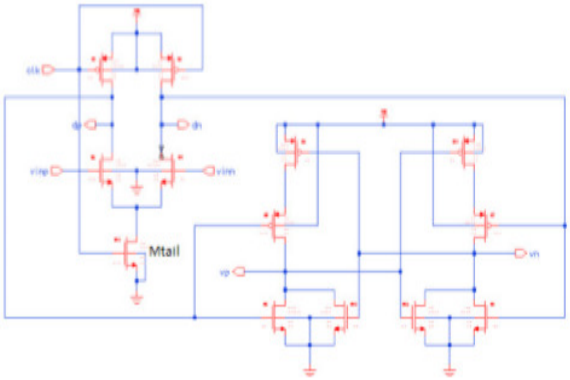

Figure 7: Circuit diagram exhibiting single clocked dual rail dynamic latched comparator.

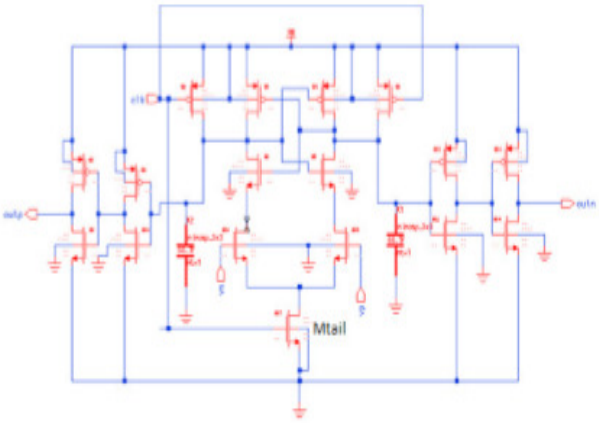

Figure 8: Schematic diagram of balance type latched regenerative comparator

The circuit of balanced type latched Regenerative comparators is depicted in Figure 8. Based on the clock input applied, the comparator works in Comparison mode and reset mode.

- In reset mode of operation clock input is given as 0V, the corresponding Mtail transistor in the comparator architecture turns OFF resulting the voltage output nodes to VDD.

- In comparison mode the Mtail transistor is ON as the clock input is equal to VDD. Therefore both the output nodes starts to discharge through the Mtail transistor. Depending on the input voltages, regeneration of latch is achieved by one of the cross coupled inverters leading the outputs to be 0 and VDD volts. In this circuit the capacitors are arranged in parallel form in order to reduce thermal noise.

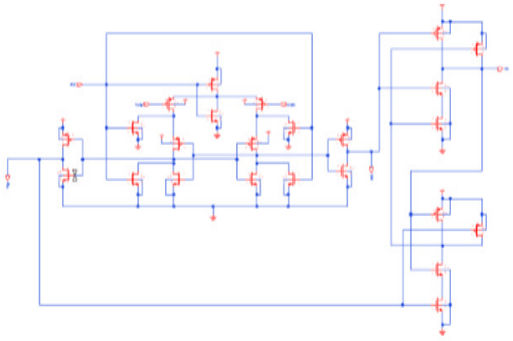

Figure 10: Schematic diagram of SR latched dynamic comparator.

The architecture of the Single Clocked dual rail dynamic comparator is demonstrated in Figure 10.The circuit operates in two phases

- In precharge phase clock is set to '0V' and in evaluation phase clock is kept at VDD. During the precharge phase, the nodes DP and DN are precharged to VDD, while the nodes VN and VP are discharged to zero volts. When the clock input raises, the Mtail transistor will be switched on resulting an input dependent differential voltage at the nodes DN and DP.
- In the evaluation phase, final output of the comparator is achieved by one of the cross coupled inverters where one of the outputs is pulled to voltage of 0v and the other output node is pulled to VDD volts. Even though dual rail dynamic comparator consumes more power when compared with single rail dynamic comparator, dual rail latched compared is chosen because it generates less kickback noise[7,8,9,10].

3. Proposed Architecture Of Latched Comparator:

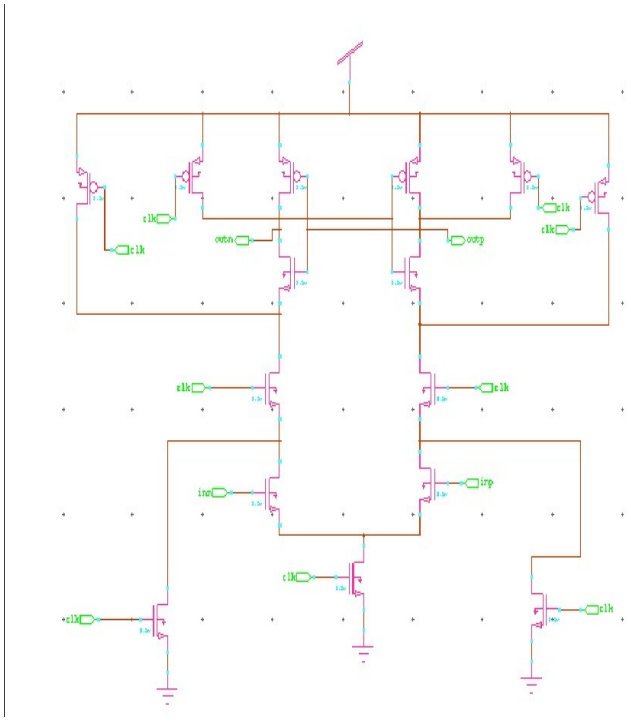

Figure 11: Proposed architecture of latched comparator

In this paper we design the latched comparator and simulate the circuit by using TANNER software. The tanner software contains four types of edits.

1. L-EDIT

2. S-EDIT

3. LVS EDIT

4. W EDIT

Firstly, we design the proposed circuit by using S EDIT.The input of the design is clock signal.

- When CLK=0 all the PMOS transistors turn ON and NMOS transistors turn OFF. In this condition the PMOS transistors act as short circuit and the output is charged to VDD.

- When CLK=1 or VDD then all NMOS transistors turns ON and PMOS transistors turns OFF. In this condition NMOS acts as short circuit and output is discharged to GND.

In this proposed architecture of latched comparator two conditions are existed. They are

- If VINP>VINN,the output node outp discharges fastly to VDD than the output node outn.
- If VINP<VINN, the output node outn discharges fastly to GND than the output node outp.

4. Simulation Results

The Transient response of the proposed comparator is depicted in the fig 12.

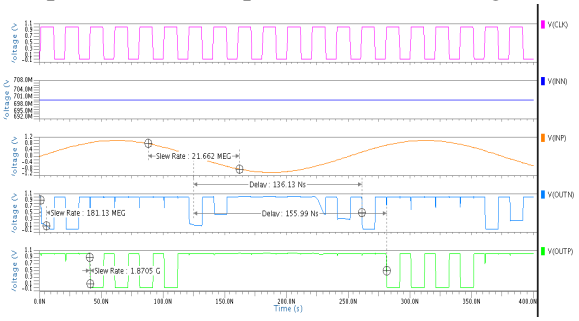

Fig 12: Transient analysis of proposed comparator

Here the comparison is done as explained in the operation of proposed comparator.

Table 1:Comparision table.

Type of comparator	Power dissipation	Kickback noise
Balanced dynamic comparator	2.63 nW	1767.6 mv
Latched comparator with SR latch	1.13 nW	1145.29 mv
Clocked dual rail comparator	6.01 nW	1239.2 mv
Proposed comparator	1.02 nW	989.9 mv

From the comparison table it is evident that proposed comparator dissipates low power and also suffers from low kickback noise when compared with the other architectures.

5. Conclusion

In this paper, the latched comparator for cardiac medical application is proposed and simulated with a supply of 1 v by using 130 nm CMOS Technology. The parameters like power dissipation and kickback noise are measured to analyze the performance of the proposed comparator. The proposed comparator consumes less power and also has low kickback noise as compared to the other architectures.

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