Implementing a 1-bit hybrid full amplifier with 22 nm CMOS technology with low power consumption

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ABSTRACT
Digital and VLSI systems rely heavily on adders. The use of arithmetic operations is crucial in digital systems. The whole study in VLSI systems is focused on reducing the transistor scale to enforce any other digital system. This suggested design is implemented by several logic system types, each of which plays a specific function in the hybrid system. This structure uses a hybrid Full Adder cell with a single bit. Using a 22-nm CMOS hybrid full adder, the proposed approach is studied. Based on the outcomes of the simulation, the suggested architecture exhibits significant power consumption efficiency. The simulation's output indicated that the data route design uses a complete adder circuit to power a low power central processor unit. This form of hybrid Full Adder increasing efficiency and mainly used in nano technology applications. This kind of adder allocates significant improvements in power and area compared with previous full adder designs.
Keywords: low power 1 bit full adder, 22 nm cmos technology, nano technology, TG Adder (TGA) and Transmission Function Adder (TFA)

1. INTRODUCTION

Today's technology reduces gate length and transistor thickness as it moves from micrometre to nanoscale scale. In VLSI systems, full adders play a significant role in enhancing the performance of digital and nano computing systems. Minimizing power consumption for digital systems requires optimization at all design stages. This article illustrates the approach of creation that incorporates the technologies for creating digital circuits, their architectural designs, and the most advanced algorithms. Arithmetic units are employed in contemporary computer applications to increase the effectiveness of adder systems. The hybrid adders highlight the significance of low power design approaches. The transistors are used as voltage controlled switches in this transistor logic.A full adder is used to different logic styles and its gives different benefits. Consequently, these different types of full adder can implement the techniques inmicroprocessor systems. The logic designstyle of Hybrid-CMOS uses more than one element full adder design. For example, this kind of adders added into the hybrid CMOS design. The different method of adders are use more than one logic design, called as hybrid-logic design style, these hybrid full adder designs is used for complex circuits and it‟s also used in nano technologyapplications. This style of logic design givesthe high efficiency and high performance of logic circuits. The one bit full adder performance is good but the performance degenerate drastically as the chain size increased. A new 1 bit hybrid full adder using different types of gates like PTs, TGs, and static CMOS logic was introduced. In this type of hybrid full adder was designed by 22nm technology. To comparing C- CMOS circuits, the hybrid structure circuit gives high speed, low power and high efficiency. Thus the hybrid logic styles deliver promising power and delay efficiency. Existing System: In existingsystem, hybrid logic style is adopted to design the full adder. Hybrid logic style used is the combination of CCMOS logic (Complementary Metal Oxide Semiconductor) and Transmission gate (TG)logic. The Circuit was implemented using Micro-wind tool in 32nm technology. It requires more power and low performance. Proposed System: The proposed system is, build A new 1 bit hybrid full adder using different types of gates like PTs, TGs, and static CMOS logic. In this type of hybrid full adder was designed by 22nm technology. When comparing to C-CMOS circuits this hybrid structure circuit work at low power and high efficiency. Thus the hybrid logic styles deliver promising power efficiency. The hybrid structure techniques are use of TGs in the architecture, TG Adder (TGA) and Transmission Function Adder (TFA).TGA and TFA FA's main benefit is not suffering from voltage loss,

low performance.

CMOS logic structure: Today CMOS (Complementary Metal Oxide Semiconductor) is the primary technology in the Semiconductor industry. Most high speed microprocessors are implemented using CMOS. Contemporary CMOS technology is characterized by: Small minimum sized transistors, allowing for dense layouts, although the interconnect limits the density. Low Quiescent Power - The power consumption of conventional CMOS circuits is largely determined by the AC power caused by the charge and discharge of capacitances:

2. LITERATURE REVIEW

The research [1] introduce that the full adder cells play a vital role in numerous VLSI circuits. Therefore, design of an energy-efficient full adder which operates reliably in submicron technologies has become a great concern in recent years. Some previously designed cells suffer from non-full swing outputs, high-power consumption and low speed issues. In this paper, two high-speed, low-power and full swing full adder circuits are designed in 90- nm CMOS technology. According to simulation results, the proposed circuits have rail to rail output signals. Also, an improvement of 12%-52%, 7%-48% and 28%-68% has been achieved in delay,power consumption and power delayproduct (PDP), respectively. In this paper[2], hybrid logic style is adopted to design the full adder. The main objective of this design is to achieve Low power and high speed. Hybrid logic style used is the combination of CCMOS logic (Complementary Metal Oxide Semiconductor) and Transmission gate (TG) logic. The Circuit was implemented using Micro-wind tool in 90nm and 180nm technology. Performance metrics of power and speed are compared with existing adder designs such as conventional CMOS adder, Transmission gate adder (TGA) and Transmission Function adder (TFA). Average Power consumption of the proposed design is found to be 1.114 µW at 90nm for 1.2V supply and 5.641 µW at 180nm for 1.8Vsupply. Delay in the signal propagation is measured as 0.011ns and 0.087ns for 90nm and 180nm technologies respectively. Thus consuming extremely low power and requires less time than existing designs for the same testing environment. Power Delay Product (PDP) is calculated as product of Power and delay values signifies energy requirement of the design. Proposed design requires 71% less energy than TFA and 81% less energy than TGA and 92% less energy than conventional CMOS adder. In modern nanotechnology and quantum computation[4], reversible logic plays a pivotal role as it has minimal impact on physical entropy. Reversible logic gates have same number of input and output hence power loss due to biterase operation can be avoided. There are many reversible logic structures which can perform different Arithmetic and logic operations as traditional or classical logic structures can do. In this paper, two reversible logic structures are proposedwhich can perform operation of addition. These logic structures namely proposed design I and Proposed design II, generate carry output signal and carry propagate signal on the basis of two reversible logic gates known as Fredkin gate and Feynman gate. Performance of proposed designs is evaluated in terms of quantum cost, constant input, garbage output and delay. It is found that proposed design II is a better choice over proposed design I and some other existing Designs. The Paper [5] discussed the comparative analysis of different Fin-FET based full adder cells designed withvarious logic styles. The logic styles usedfor implementation of Fin-FET based 1-bit full adder are Complementary MOS (CMOS), Transmission Gate (TG) and Complementary Pass Transistor Logic (CPL). The simulations have being done at 10nm, 20nm and 32nm technology node for all full adder cell designs. PTM models for multi-gate transistors (PTM-MG) low powerare used for simulations. The performance parameters that were measured, analyzed and compared are average power, leakage power, delay, and energy. It is observed thatless power is consumed in Transmission Gate (TG) based full adder than the Convention full adder and complementary pass-transistor logic (CPL) based full adder in 10nm technology node. Also, found reduction in delay, EDP, and PDP in TG based full adder compared to other cell designs. The paper [6] very large-scale integrated circuit (VLSI) design, based on today‟s CMOS technologies, are facing various challenges. Shrinking transistor dimensions, reduction in threshold voltage, and lowering power supply voltage, cause new concerns such as high leakage current, and increase in radiation sensitivity. As a solution for such design challenges, hybrid MTJ/CMOS based

design can resolve the issue of leakage power and bring the advantage of non-volatility. However, radiationinduced soft error is still an issue insuch new designs as they need peripheral CMOS components. As a result, these magnetic-based circuits are still susceptive to radiation effects. This paper proposes a radiation hardened and low power magnetic full-adder (MFA) for advanced microprocessors. Comparing with the previous work, the proposed MFA is capable of tolerating any particle strike egardless of the induced charge. Besides, our MFA circuit offers a lower energy consumption in write operation as comparedwith previous counterparts. They also suggest an incremental modification to the proposed MFA circuit to give it the advantage of full nonvolatility for future nonvolatile microprocessors.

3. DESIGN AND IMPLEMENTATIONWorking Functionality

A hybrid FA was used in this process of using PTs, TGs and C-CMOS logic. Themajor capability of the hybrid adder circuitis the most important resources, and the researchers are trying to save these kind of logic styles. This paper represents the power dissipation properties in CMOS circuits are switching operation, transistor size, intermediate node capacitances (diffusion, gate and wiring capacities). For avoiding complicated structure a recent method is invented for hybrid logic circuits to analysesthe circuit behavior. The main purpose of this paper is used to different kind of logic styles, these logic styles improve the hybrid structure. In particular, when operating on a normal tool, the power consumption is too long and high delay error occurs. Foravoiding this kind of error using spice tool which is implements the less size of transistors and reducing power consumptionand delay etc. The hybrid structuretechniques are possible to increase the timing analysis of nano technologies. Researchers are currently using hybrid design approach that makes use of the favorable aspects of multiple logic types within the same full adder unit. In use of TGs in the architecture, TG Adder (TGA) and Transmission Function Adder (TFA).TGA and TFA FA's main benefit is not suffering from voltage loss, lowperformance.

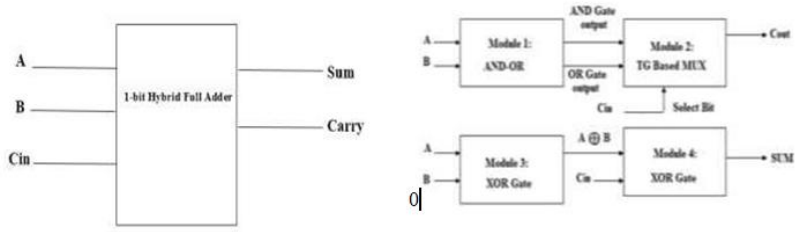

Figure 1: Symbol diagram for one bit Hybrid fulladder

The hybrid full adder has two types of combination there are static and dynamic. The main focus of hybrid logic adderresearch includes different types of adderbased on separate types of logic designs is expressed. This kind of adders is basically used in nano technology implementation in recent circuits.

Full Adder Design

The hybrid full adder design using single bit implementation is designed in this paper. For comparing previous conventional adders, this hybrid structure has include low power consumption, high speed and highefficiency. The main approach of proposed system represents in 22 nm technology.

Hybrid-CMOS Logic Design

The hybrid FA architecture is classified into following terms, and it represents carry and sum generation parts. The main achievement of vlsi design circuits is to be reducing the size of transistor and increases high speed and less power. The proposed method exhibits the reduced size with 22nm CMOS technology with 0.8V power supply.The basic block diagram of proposed method is mentioned in the following block diagram.

The system has been proposed in this research considering a new hybrid FA using different types of transistor logic styles. The proposed full adder design was implemented by 22nm technology. To determine the reliability, a comparative review of the design's output parameters was carried out with twenty existing FA designs with 0.4 V to 1.2 V power supply.

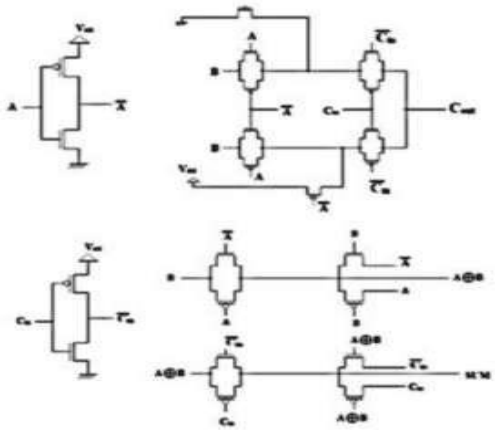

Figure 2: Full Adder Carry and Sum Generation

Compared to the existing FAs, the existing full adder showed the performance in different ranges of power supply. The carry and sum generation is represented in the following circuit diagram. The proposed method implemented by using CMOS technology which reduces the delay, especially this structure is used for low power design circuits. The proposed full adder is developed by 22nm technology. The supply voltage is reduced by 0.8v itincreases the efficiency of the digital circuits.

SIMULATION AND RESULTS

In this CMOS technology simulation wasconducted using 22 nm in order to analyseV and I performance parameters. The previous conventional adders could operate is 32 nm technology with a minimum supply voltage of 0.8 V. The proposed system results show that the FA gained simulation results on 0.8V supply voltage. The proposed hybrid full adder results showthat the higher efficiency in power. The input and output simulation is mentioned as following diagram.The proposed full adder will work is 22 nm technology with a minimum supply voltage of 0.8 V.

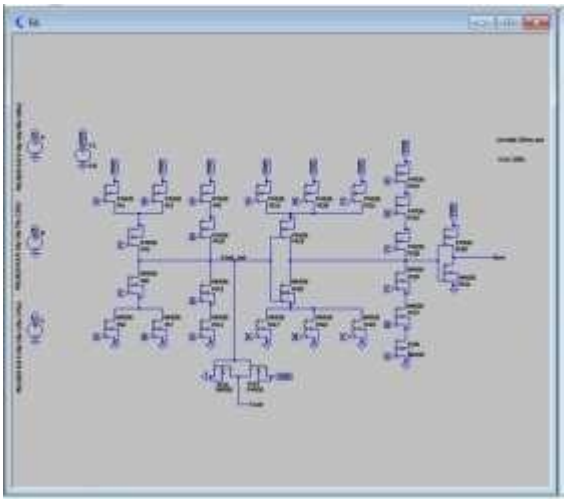

Fig: 3-Bit Full Adder using 32nm CMOSTechnology

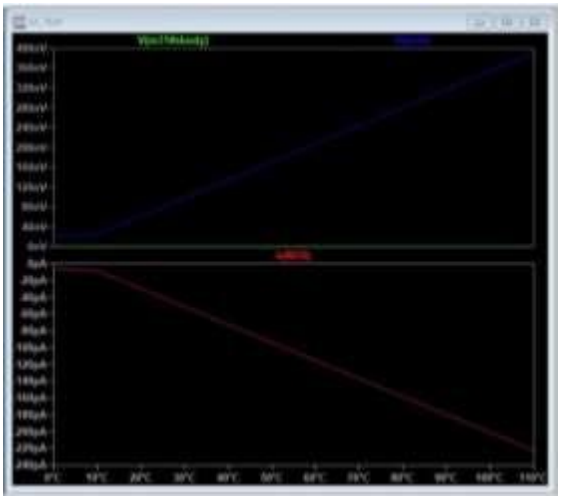

Fig: 4-Bit Full Adder Using 32nm CMOSTechnology T v_s V and T v_s I graphs

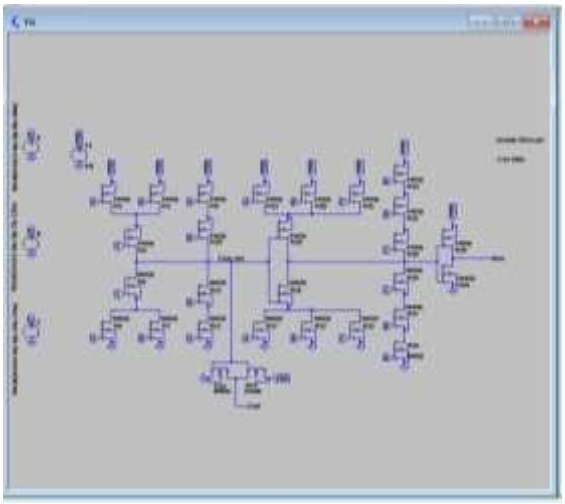

Fig: 5-Bit Full Adder Using 22nm CMOSTechnology with adder output

Fig: 6-Bit Full Adder Using 22nm CMOSTechnology T v_s V and T v_s I graphs

From The above figures deeply mentionedthe voltage and current analysis:
So power value for 32nm 1-bit full adder is120nv x 50ua=120 x 10^{-9} x 50 x 10^{-6} =600pw
So power value for 22nm 1-bit full adder is50nv x 180 ua=50 x 10^{-9} x 180 x 10^{-6} =900pw
The 22nm 1-bit full hybrid adder givespromising power performance in this circuit.

CONCLUSION

A one bit hybrid Full Adder design has implemented using low power consumption less delay and high efficiency performance. Features of the design proposed were compared with existing FAs. The hybrid circuits is developed by different logic styles. The proposed Full Adder indicateshigher performance in speed and power, andalso used to implement the low power design circuits. The power consumption of l.lO551iW was found with 0.8-V supply at 22-nm technology, and 7.0415ps should be supplied with low delay. The proposed adder is suitable for both CMOS and nano technology based VLSI circuits and systems. To validate the result, simulation has been implemented by using spice tool. The performance of this proposed method was implemented for less power consumption circuits which is used in nano technology applications. And the hybrid design logic circuits mainly used for customizing design circuits with low power and delay with high efficiency.

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